Nonideal Effects in SC circuits

Gabor C Temes
School of EECS
Oregon State University

Rev. 9/4/2011

Oregon State University OSU

temes@ece.orst.edu

Components and Nonidealities

- **Switches:**

Nonzero “on”-resistance

Clock feedthrough / charge injection

Junction leakage, capacitance

Noise

- **Capacitors:**

Capacitance errors

Voltage and temperature dependence

Random and systematic variations

Leakage

- **Op-amps:**

DC offset voltage

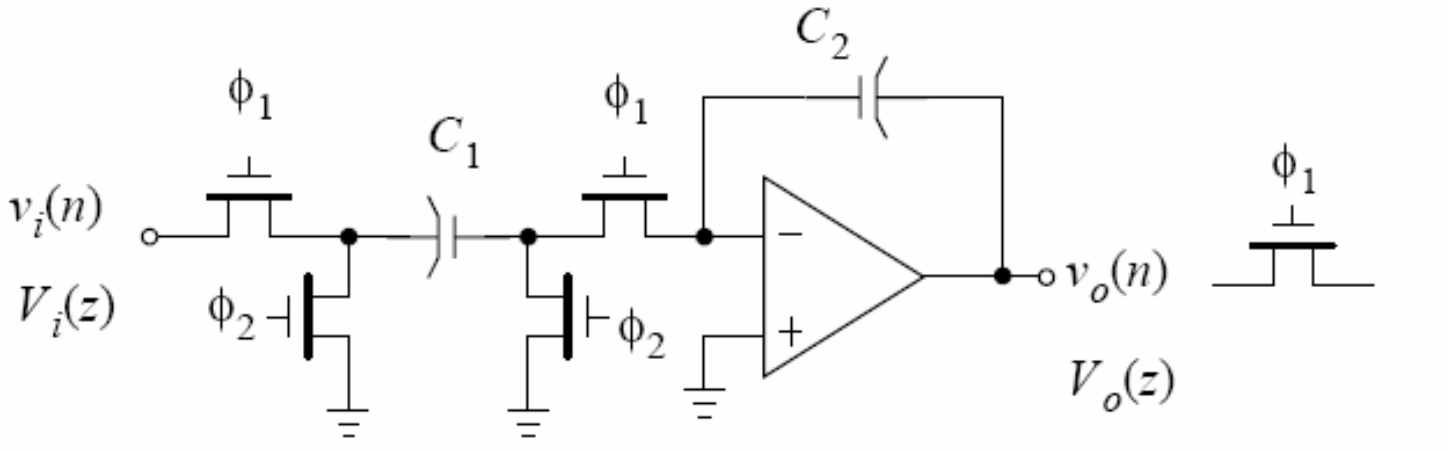
Finite dc gain

Finite bandwidth

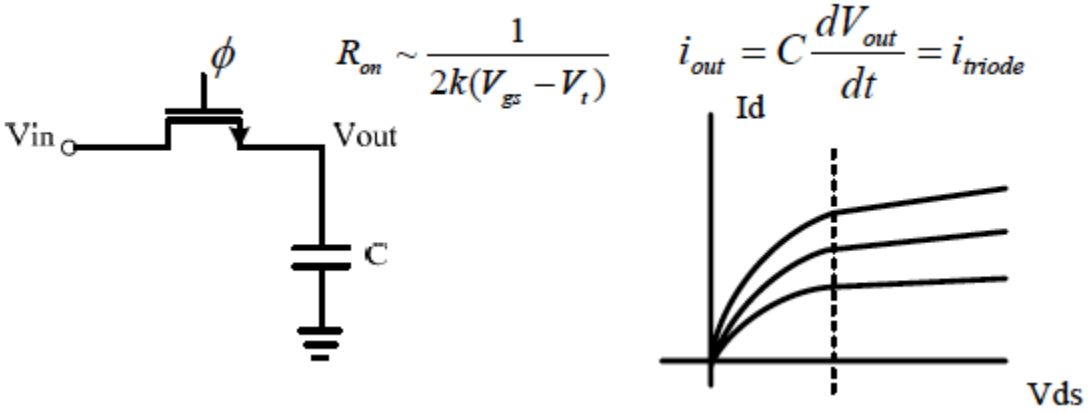
Nonzero output impedance

Noise

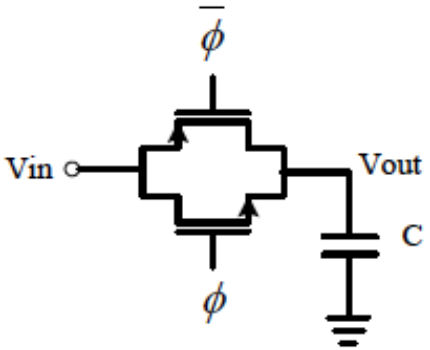
Switched-Capacitor Integrator



Nonzero Switch "On"-Resistance

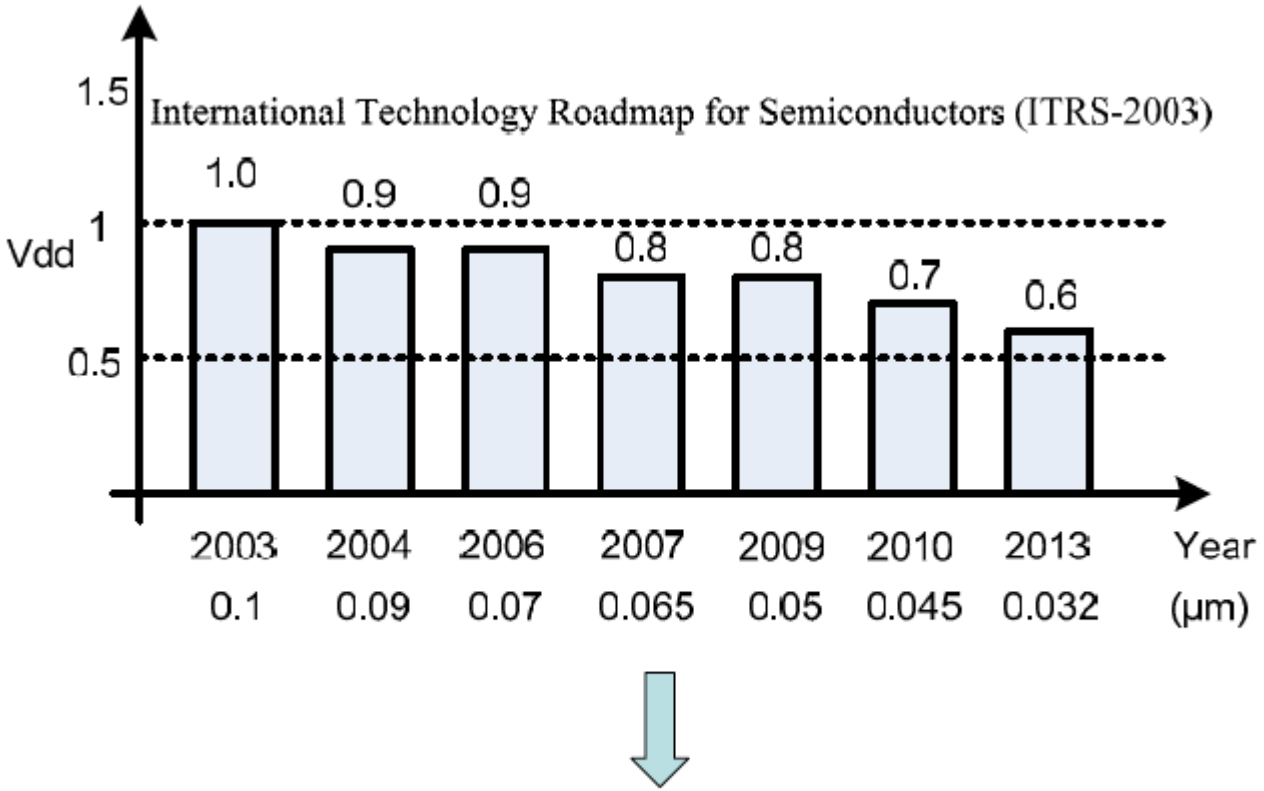


C is charged exponentially. Time constant must be sufficiently low. Body effect must be included!



To lower on-resistance and clock feedthrough: CMOS gate; Wp,Lp =Wn,Ln. For settling to within 0.1%, $T_{settling} > 7R_{on}C$ (worst-case R_{on}).

Digital CMOS Scaling Roadmap



Want analog circuit to operate at low supply voltage

Predicted Dimensions

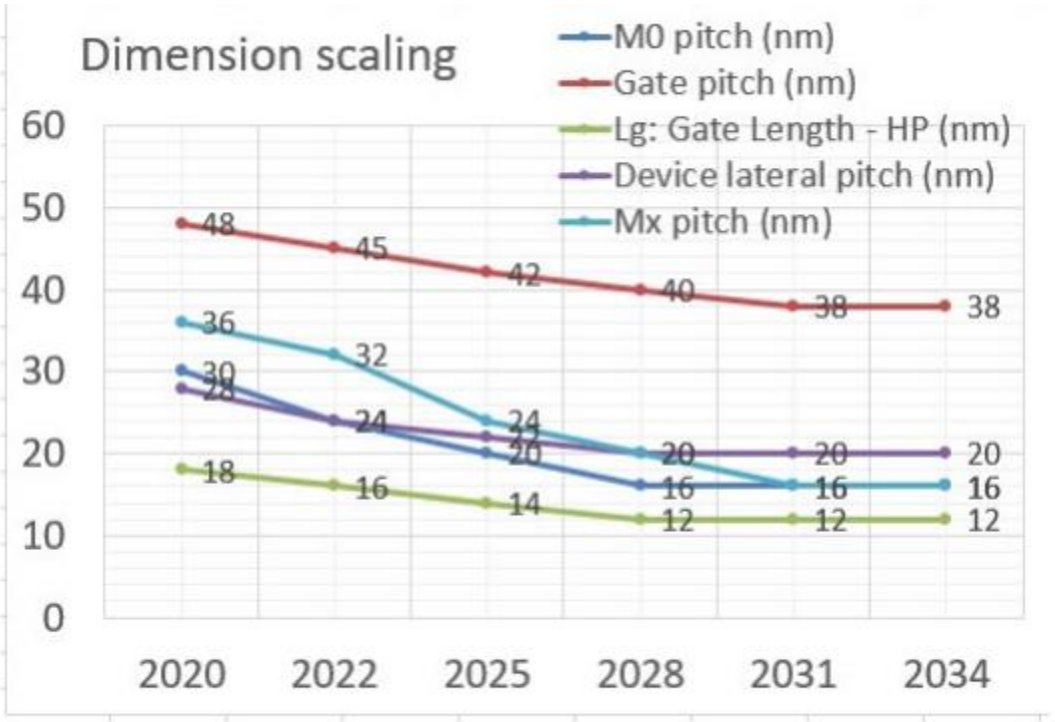
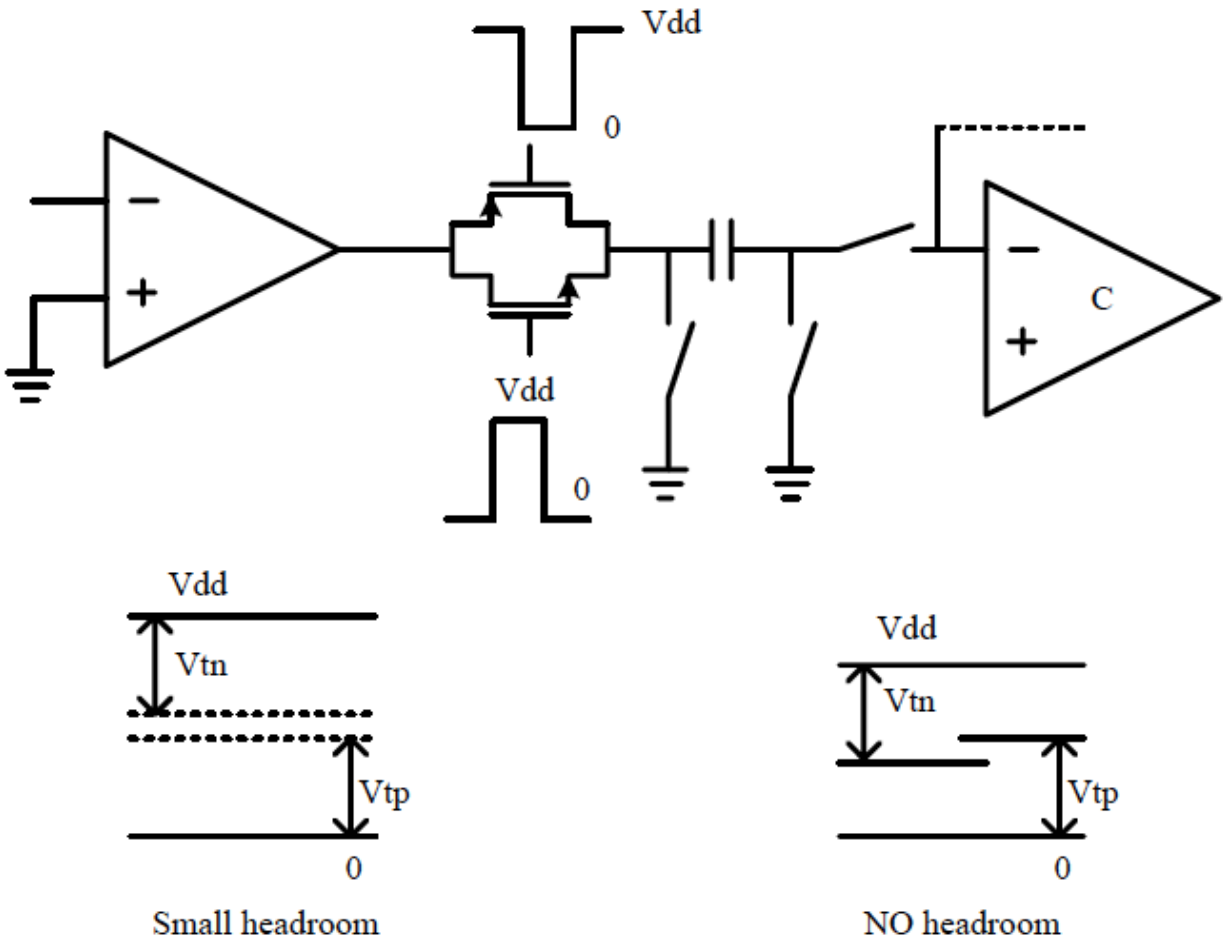


Figure MM-2 Projected scaling of key ground rules

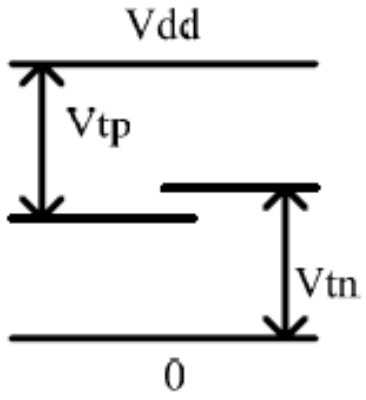
Floating Switch Problem in Low-Voltage



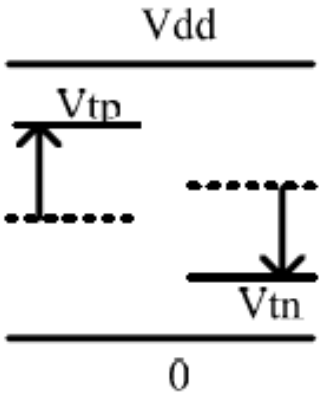
•*FORBIDDEN REGIONS FOR SIGNAL*

Using Low-Threshold Transistors

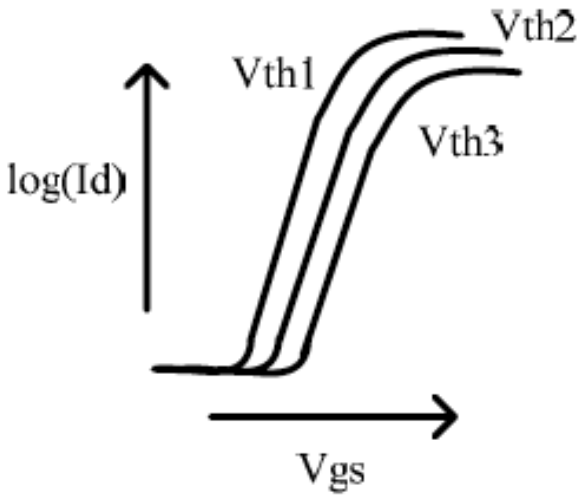
- Precise control over process and temperature difficult
- Switch leakage worsens as threshold voltage is lowered (i.e. hard to turn off)



NO headroom



Increased headroom



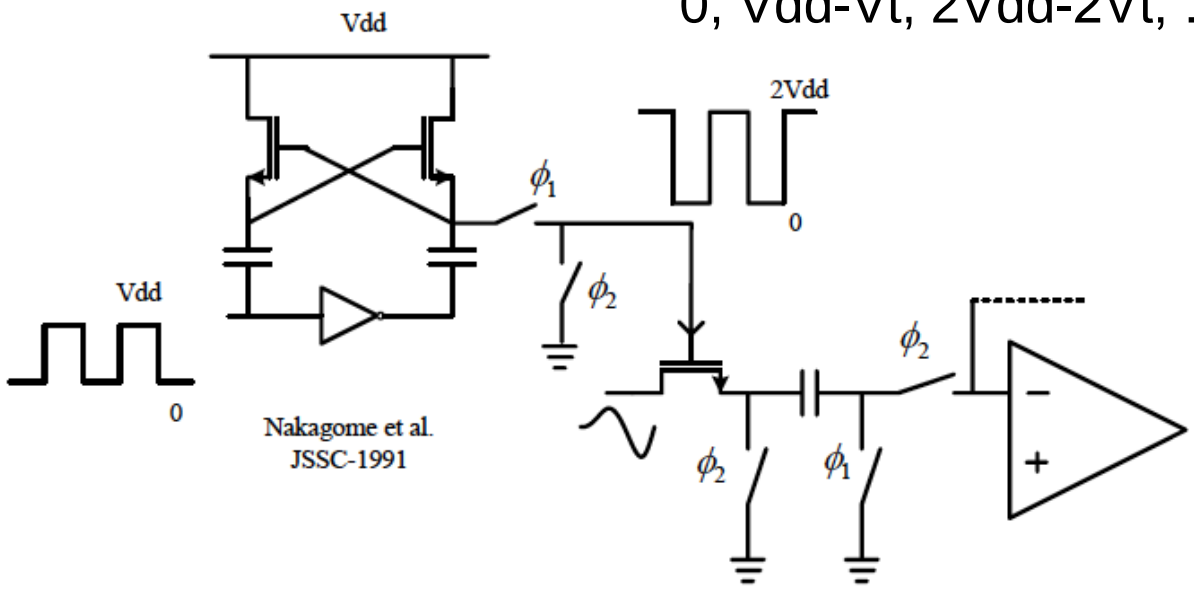
Using Clock Voltage Booster

- Boosted clock voltage (e.g. 0 → 2Vdd) is used to sufficiently overdrive the NMOS floating switch – useful in systems with low external power supply voltage and fabricated in high-voltage CMOS process

  Battery,harvested energy may be used!

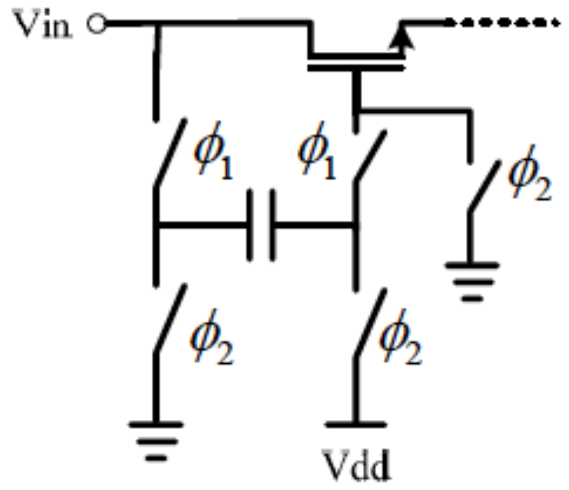
  → Voltage limitation is violated in low-voltage CMOS

0, Vdd-Vt, 2Vdd-2Vt, … 2Vdd



Using Boostrapped Clock

Abo et al., JSSC-1999
Steensgaard, ISCAS-1999
Singer et al., ISSCC-2000
Dessouky et al., JSSC-2001
(fast) Hernes et al., ISSCC-2004



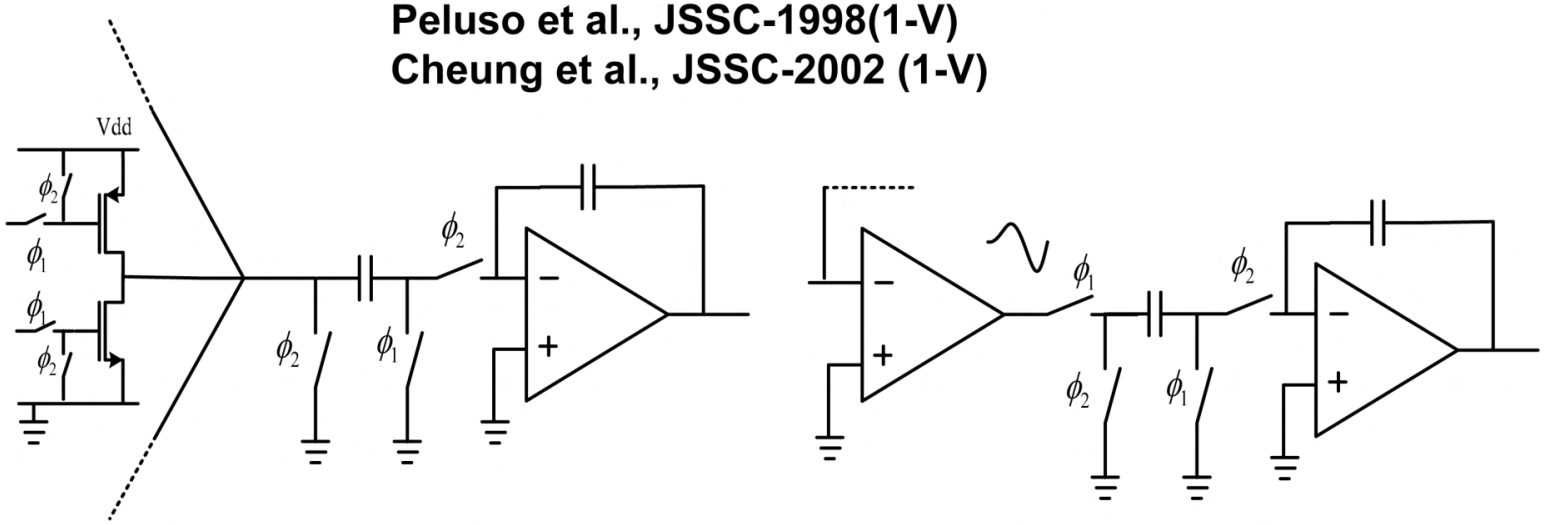
- Principle: pre-sample Vdd before placing it across Vgs (various low-voltage issues complicate implementation)
- Input sampling such as this can be used for low-voltage CMOS or for high-linearity sampling
- No fundamental or topological limitation on higher input signal frequency vs. sampling frequency

•*BUT BREAKDOWN, ADDED SWITCH TURN-ON PROBLEM.*

Switched-Opamp Technique

- Floating switch is eliminated
- Opamp output tri-stated and pulled to ground during reset ϕ_2
  → Slow transient response as opamp is turned back on during ϕ_1

Crols et al., JSSC-1994(1.5-V)
Peluso et al., JSSC-1997(1.5-V)
Baschirotto et al., JSSC-1997(1-V)
Peluso et al., JSSC-1998(1-V)
Cheung et al., JSSC-2002 (1-V)



Switched-opamp integrator **Conventional integrator**

Switched-Opamp Example

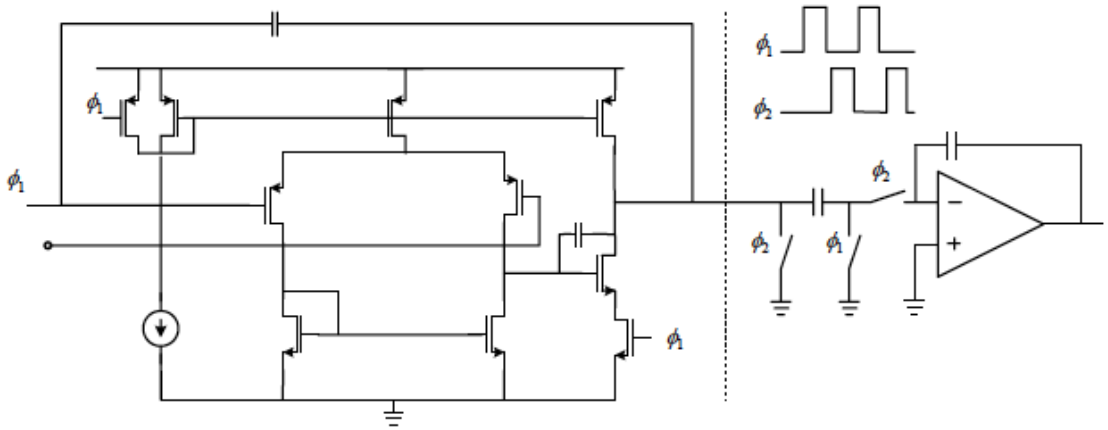
Crols et al., JSSC-1994

Peluso et al., JSSC-1997

The entire opamp is turned off during ϕ_2.

Demonstrated 1.5-V operation (ΔΣ)with Vtn=|Vtp|=0.9V.

115kHz at -60dB THD & 500kHz at -72dB THD.



→ **Baschirotto JSSC-1997: 1-V operation**

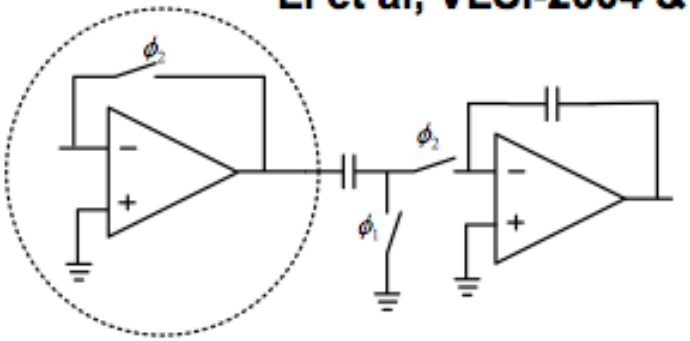
→ **Peluso JSSC-1998: 0.9-V operation**

1.8MHz at -40dB THD

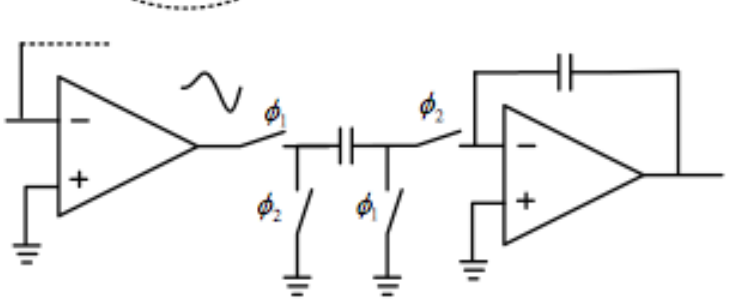
Cheung et al., JSSC-2002(1-V)

Opamp-Reset = Unity-Gain Configuration

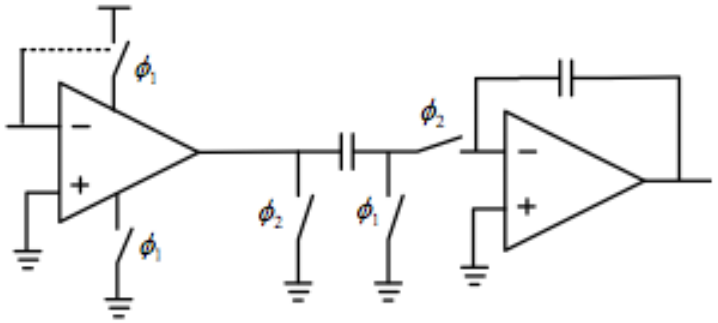
Bidari et al., ISCAS-1999
Keskin et al, ESSCIRC-2001 & JSSC-2002
Chang et al, CICC-2002 & JSSC-2003
Chang et al, VLSI-2003 & TCAS1-2005
Li et al, VLSI-2004 & JSSC-2005



- **High speed operation**
- **Free of reliability issues**



Conventional integrator

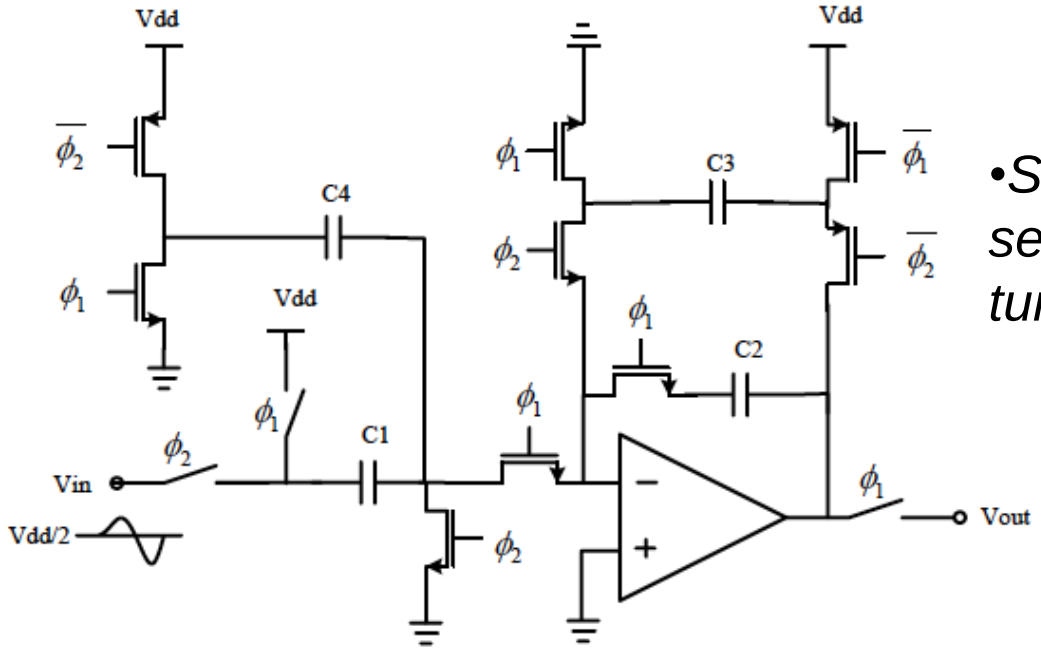


Switched-opamp integrator

Floating Reference Avoids Fwd Bias

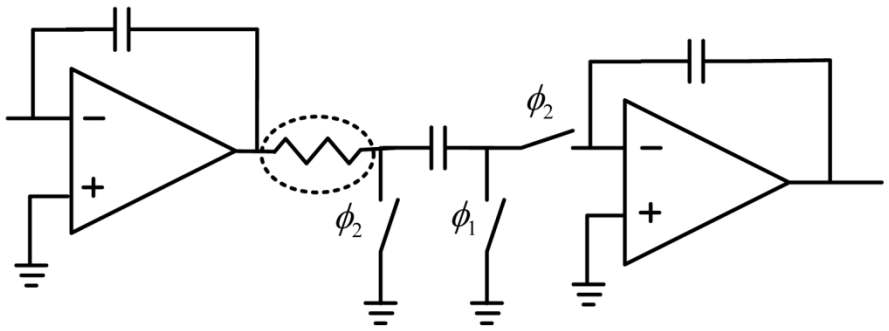
- C3 is precharged during ϕ_1
- C3 (floating reference) in feedback during ϕ_2
- DC offset circuit (C4=C1/2) compensates for Vdd reset of C1

→ effective virtual ground = Vdd/2



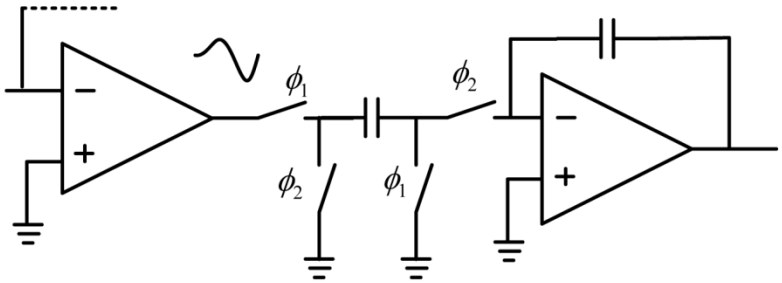
•Simpler: 2 switches in series with C2, grounded turned off first.

Switched-RC = Resistor Isolation

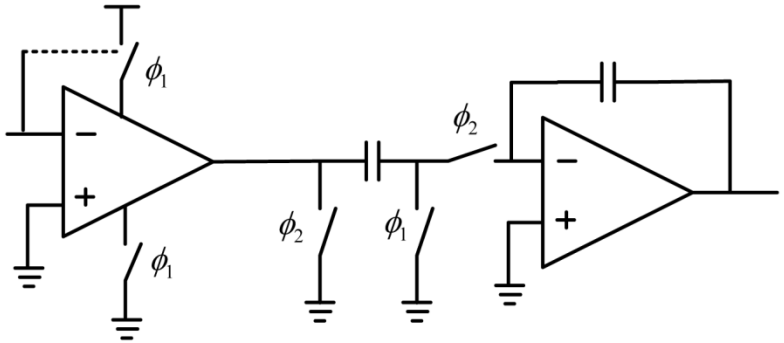


- **No floating switch**
- **Highly linear sampling**
- **Free of reliability issues**

•*R must be chosen properly.*



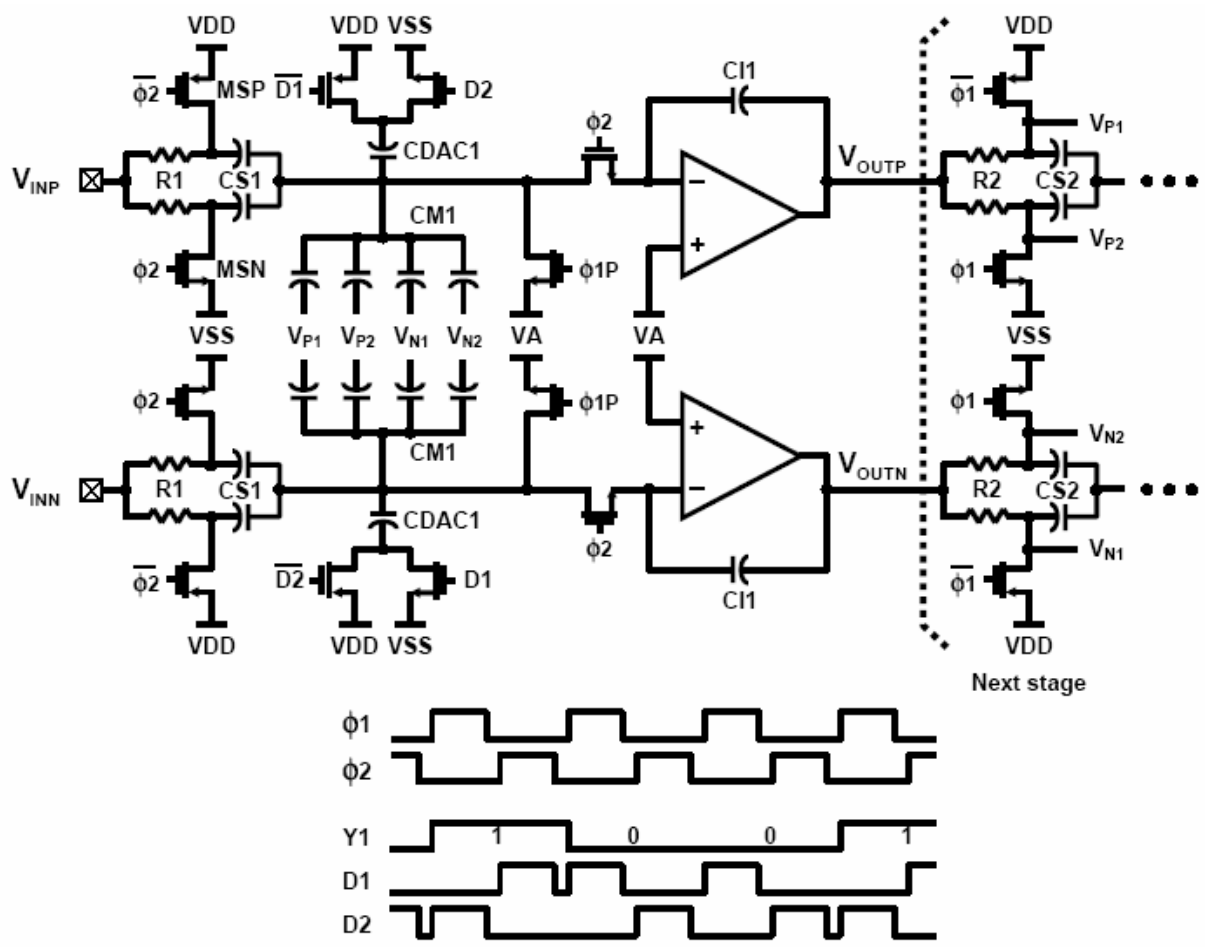
Conventional integrator



Switched-opamp integrator

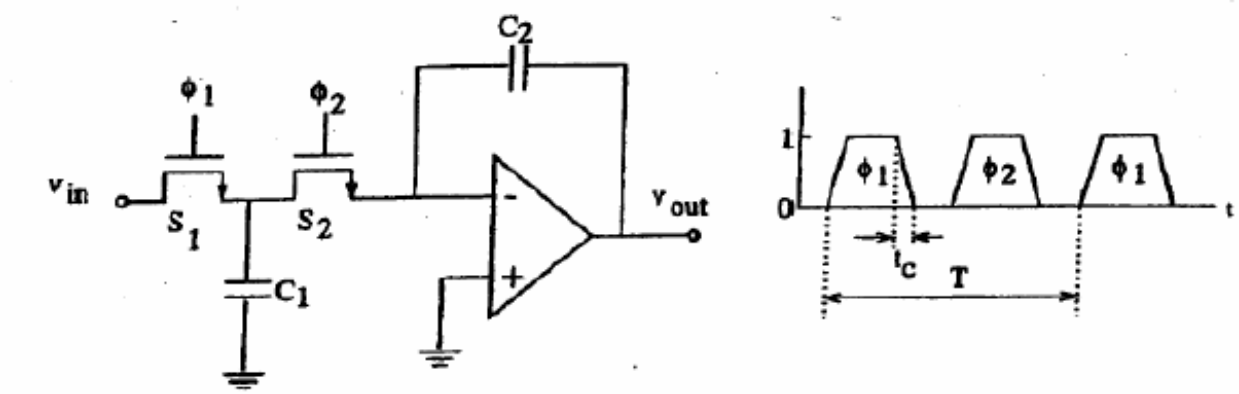
Switched-RC = Resistor Isolation

Ahn et al., ISSCC-2005 Paper 9.1

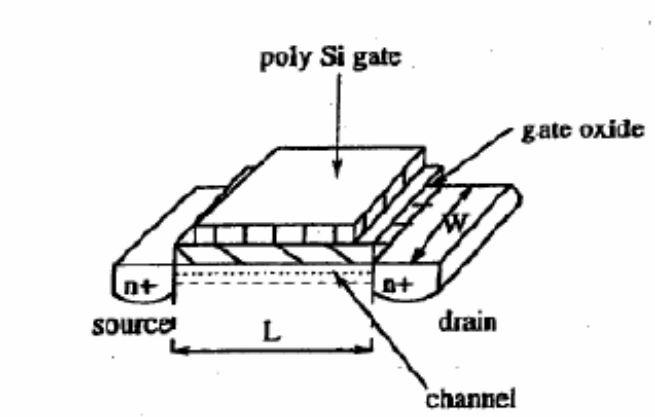


Charge Injection (1)

- Simple SC integrator



S1 structure



Charge Injection (1) (Cont'd)

- The lateral field is v/L , the drift velocity is $\mu v/L$. Therefore, the current is

$$i = q_{ch} \cdot \mu \cdot v / L^2$$

- The on-resistance is

$$R_{on} = v / i = L^2 / (q_{ch} \cdot \mu)$$

- and hence

$$R_{on} \cdot q_{ch} = L^2 / \mu$$

holds.

Charge Injection (2)

From device physics,

$$q_{ch} = -W \cdot L \cdot C_{ox} \cdot (V_{dd} - v_{in} - V_{tn})$$

Unless S1 is in a well, connected to its source, Vtn depends on Vin, so qch is a mildly nonlinear function of Vin.

When S1 cuts off, part of qch(qs) enters C1 and introduces noise, nonlinearily, gain and offset error.

To reduce qs, choose L small, but and Ron large. However, for 0.1% settling

$$R_{on} \cdot C_1 < T/14 = 1/(14 f_c)$$

Hence

$$q_{ch,\min} = L^2/(R_{on,\max} \cdot \mu) = 14 \cdot L^2 \cdot f_c \cdot C_1/\mu$$

and

$$v_{err,\min} = d \cdot q_{ch,\min}/C_1 = 14 \cdot d \cdot L^2 \cdot f_c/\mu$$

Pedestal voltage

where $d = q_s/q_{ch}$

Clock Feedthrough

Capacitive coupling of clock signal via overlap Cov between gate and source. The resulting charge error is

$$q_{ov} = -V_{dd} \cdot C_{ov} \cdot C_1 /(C_1 + C_{ov})$$

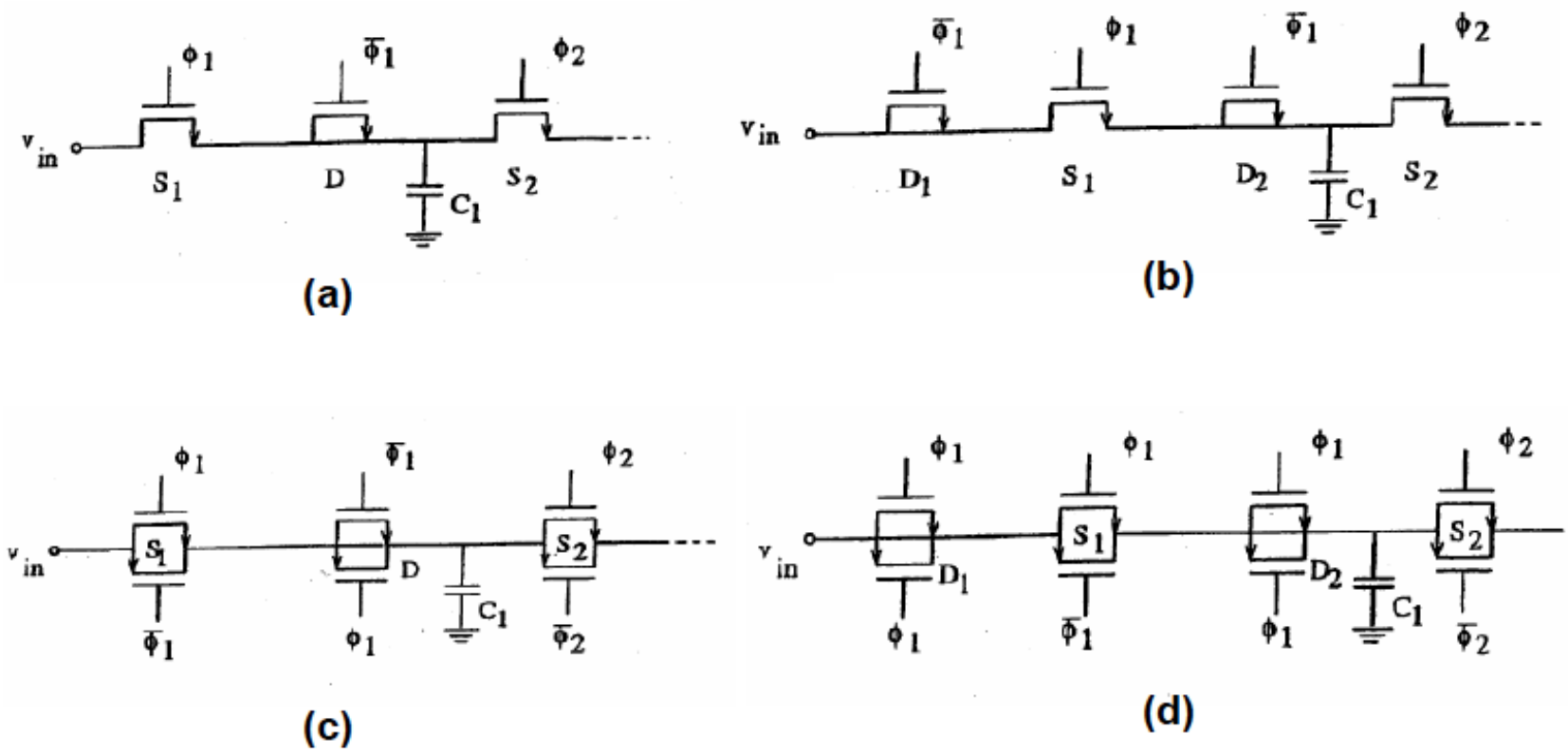
It adds to qs . Usually, $|q_{ov}| << |q_s|$

Linear error .

Same for S_1 and S_2.

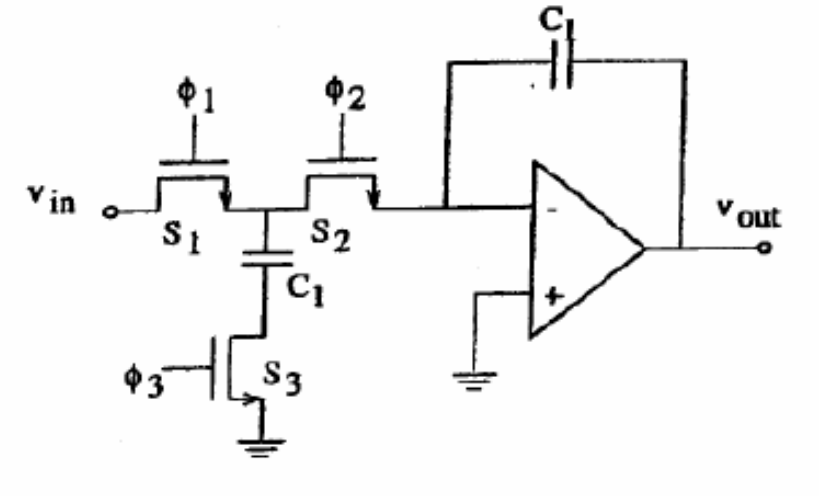
Methods for Reducing Charge Injection

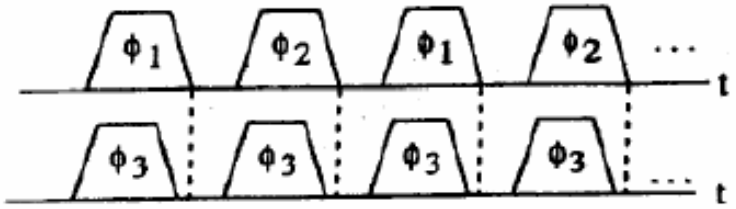
- Transmission gates: cancellation if areas are matched. Poor for floating switches, somewhat better for fixed-voltage operation.
- Dummy devices: better for d~0.5.



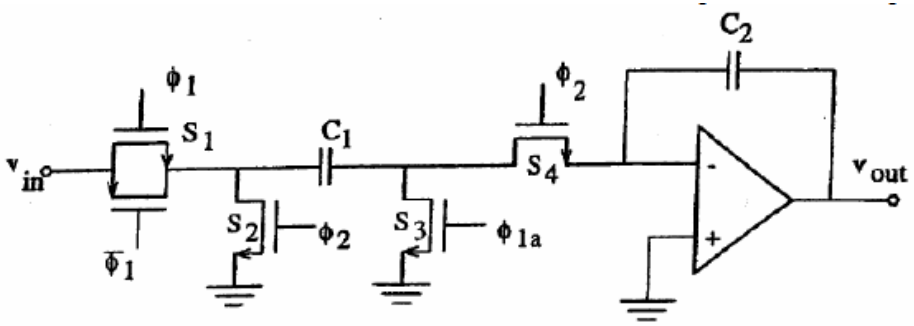
Advanced-Cutoff Switches

- Signal-dependent charge injection leads to nonlinear distortions; signal-independent one to fixed offset. Advanced-cutoff switches can reduce signal dependence.

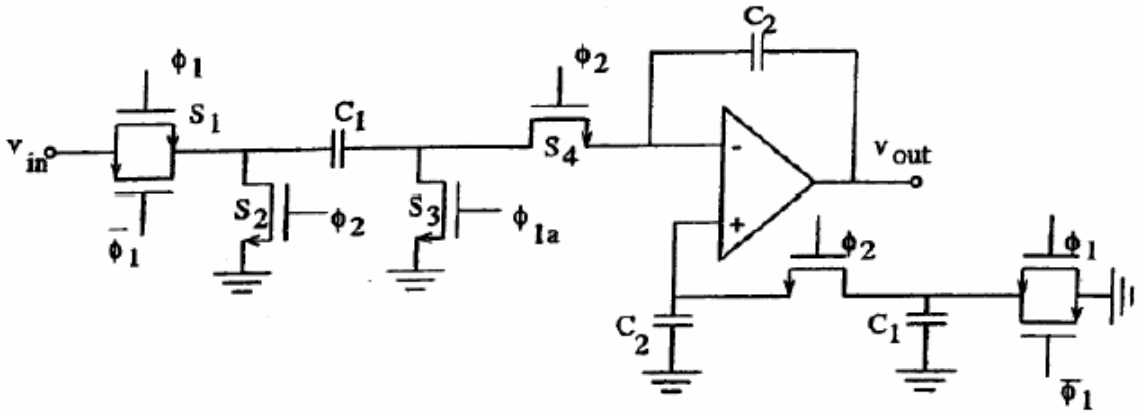




Advanced-Cutoff Switches (Cont'd)

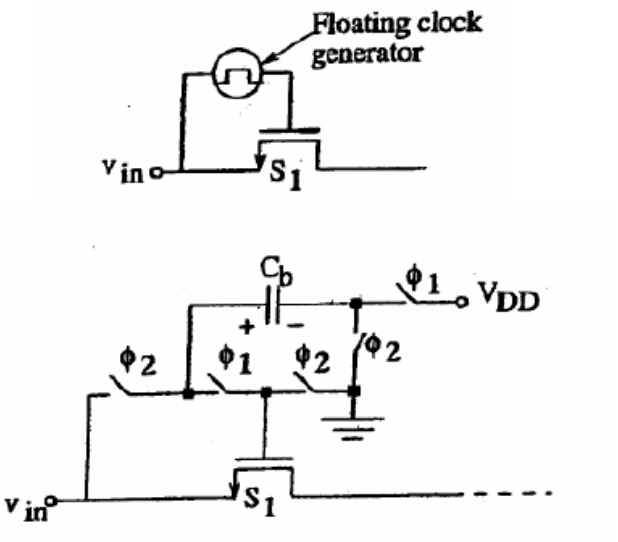


- Remaining charge injection is mostly common-mode in a differential stage.
- Suppressed by CMRR. In a single-ended circuit, it can be approximated by dummy branch:



Floating Clock Generator

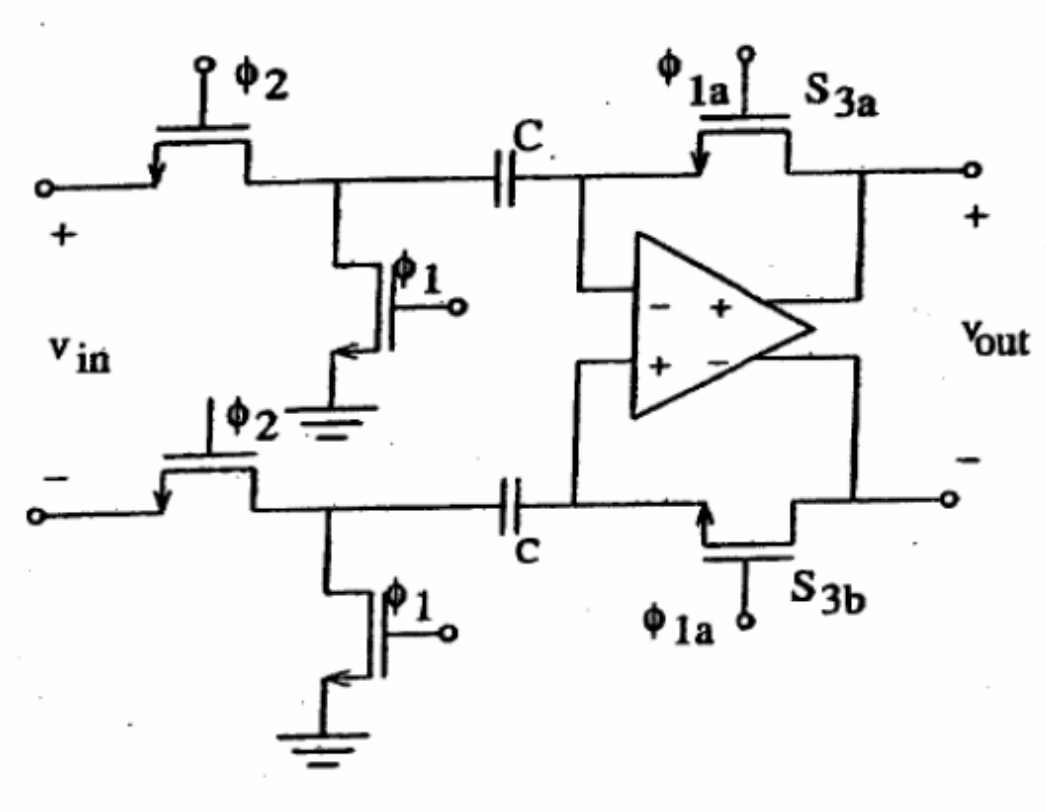
- To reduce signal dependence, reference the clock signal to vin:



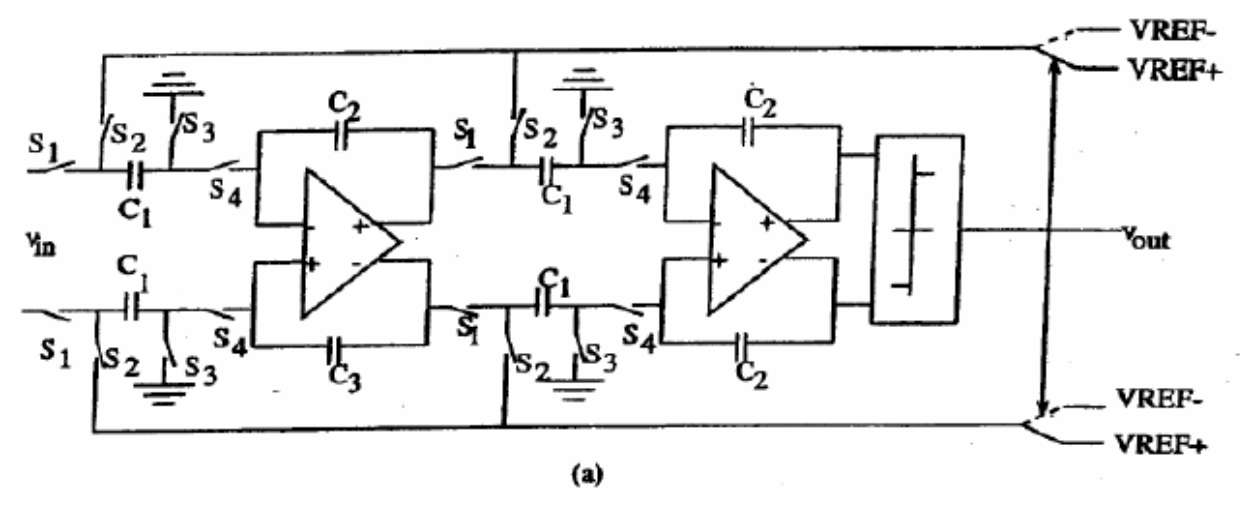
- This makes Ron also signal independent, so the settling is more linear. Clock feedthrough remains signal dependent, but it is a linear effect anyway. Better phasing : precharge Cb to VDD during phase 2, connect to vin during phase 2.

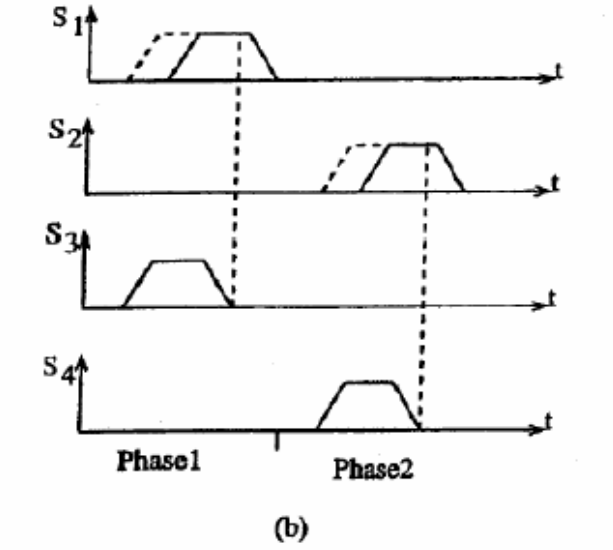
Charge Injection in a Comparator

- Remains valid if input phases are interchanged.

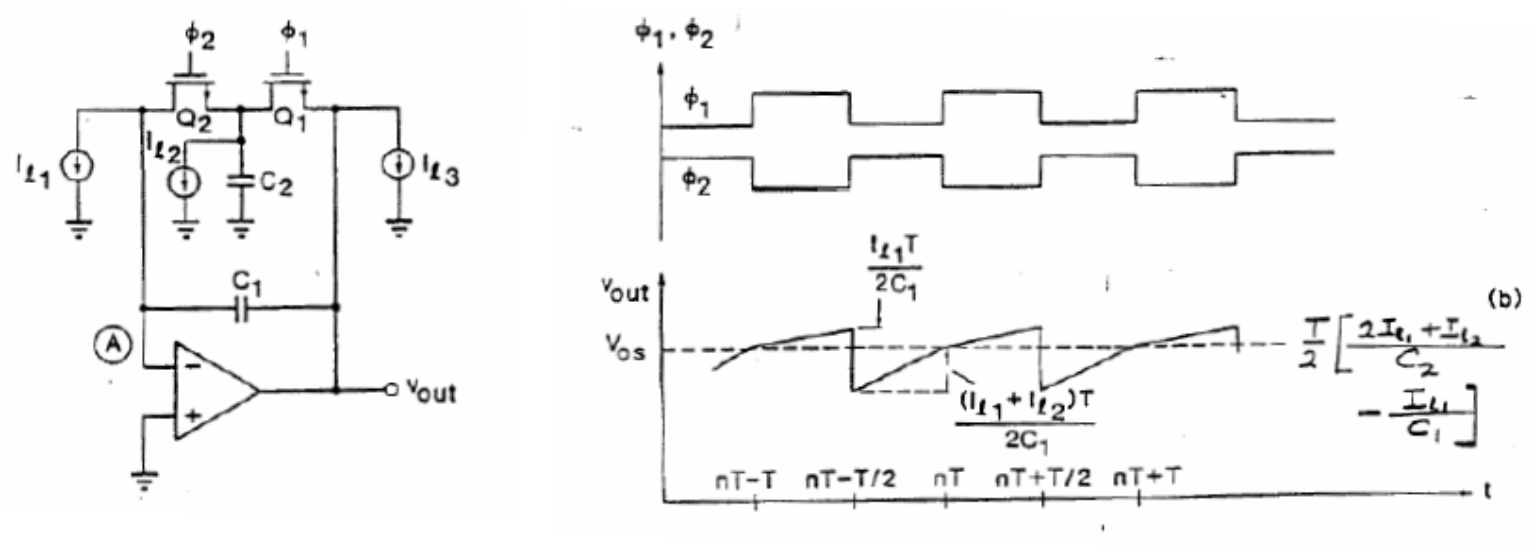


Delta-Sigma ADC





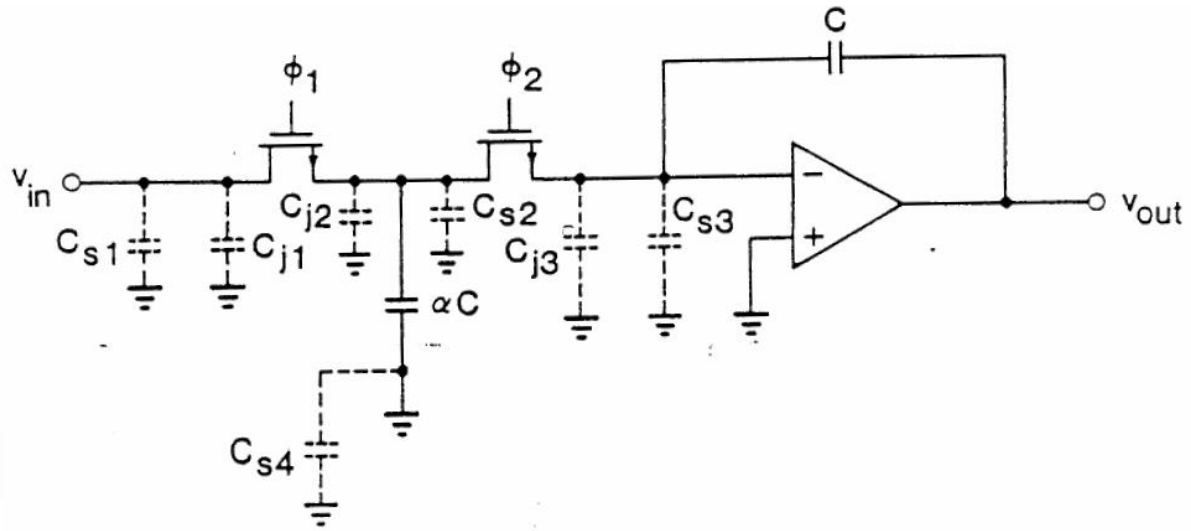
Junction Leakage



- I ~10 pA/mil^2 , 0.4pA/5μ x 5μ but doubles for each 10° C.
- fmin ~ 100Hz at 20° *C*, but 25KHz at 100° C.
- Fully differential circuit and Martin compensation converts it to common-mode effect.

Capacitances Inaccuracies

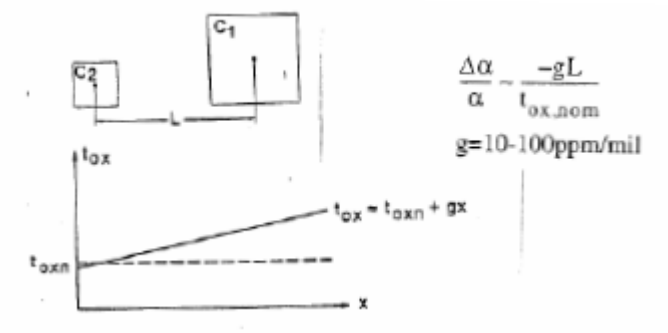
- Depends only on C ratios. Strays are often p-n junctions, leading to harmonic distortion also. For stray-sensitive integrator, all strays should be < 0.1% of *αC.*



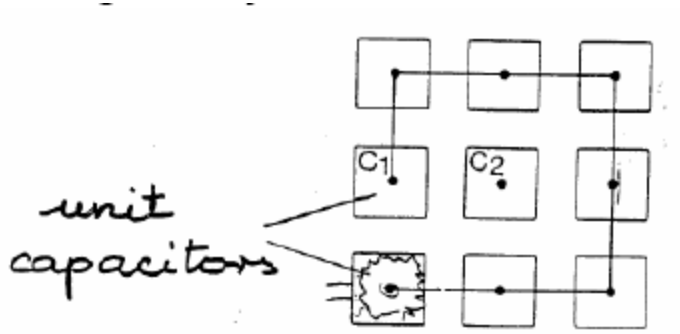
- *ΔC* can be systematic or random. Random effects (granularity, edge effects, etc.) cannot be compensated, but systematic ones can, by unit-capacitor/common-centroid construction of *αC* and C.

Capacitances Inaccuracies (Cont'd)

- Oxide gradient



- Common-centroid geometry



Compensated C1/C2 against linear variations of Cox, and edge related systematic errors (undercut, fringing)

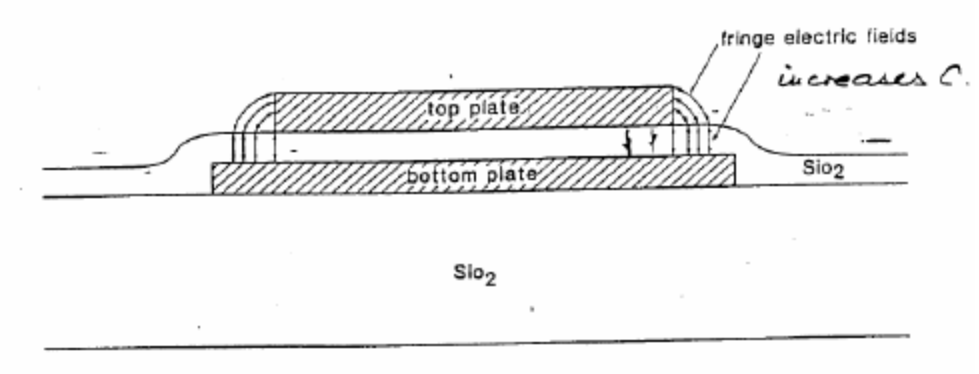
Capacitances Inaccuracies (Cont'd)

- Voltage and temperature coefficients

$$\gamma_v^c = \frac{1}{C}\frac{\partial C}{\partial v} \quad \textbf{usually} \quad \left|\gamma_v^c\right| \sim 10\,ppm/V$$

$$\gamma_T^c = \frac{1}{C}\frac{\partial C}{\partial T} \quad \textbf{usually} \quad \left|\gamma_T^c\right| \sim 20\,ppm/V$$

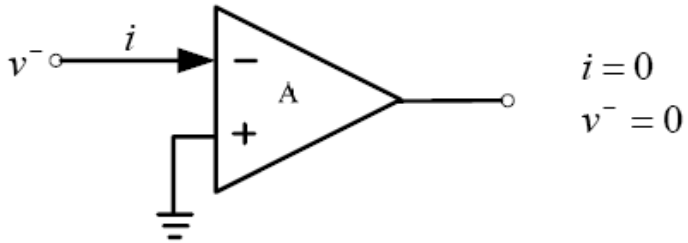
Smaller for ratios, especially for common-centroid layout:



Fringing, undercut: systematic edge effects. Reduced by commoncentroid geometry, since perimeter/area ratio is the same for C1 and C2, $\Delta C \propto perimeter$, $C \propto area$

OPAMP Input Offset

- In most analog IC, the active element is the opamp. It is used to create a virtual ground (or virtual short circuit) at its input terminals:



- This makes lossless charge transfer possible. In fact, in a CMOS IC, *i≈0* but *v≠0* due to offset, 1/f and thermal noise and finite opamp gain A. Typically, |*v*|=*5-10mV*. This affects both the dc levels and the signal processing properties. The effect of *v* is even more significant in a low-voltage technology where the signal swing is reduced, and A may be low since cascoding may not be available.

Techniques for Reducing the Effect of Imperfect Virtual Grounds

- Autozeroing or Correlated Double Sampling Schemes:

  Scheme A: Stores and subtracts *v* at the input or output of the opamp;

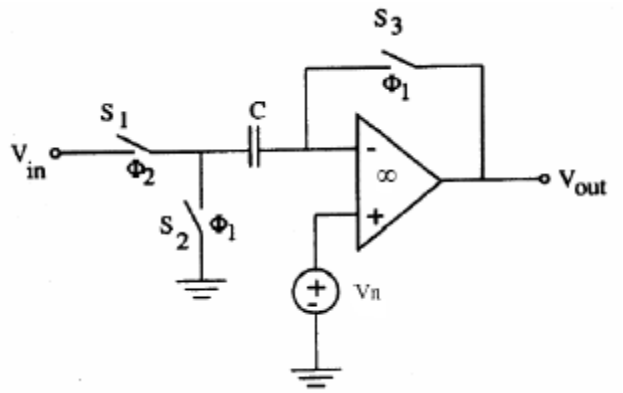
  Scheme B: Refers all charge redistributions to a (constant) *v* instead of ground;

  Scheme C: Predicts and subtracts *v*, or references charge manipulations to a predicted.
- Compensation using extra input: An added feedback loop generates an extra input to force the output to a reset value for zero input signal.
- Chopper stabilization: The signal is modulated to a “safe” (low-noise) frequency range, and demodulated after processing.
- Mixed-mode schemes: Establish a known analog input, use digital output for correction.

Circuits Using Autozeroing

- Comparators
- Amplifiers
- S/H, T/H, delay stages
- Data converters
- Integrators
- Filters
- Equalizers

Simple Autozeroed Comparator



Nonidealities represented by added noise voltage:

$$v_n = v^- = V_{os} + v_{1/f} + v_{thermal} - \mu v_{out}; \qquad \mu = 1/A_{opamp}$$

Input-referred noise at the end of interval:

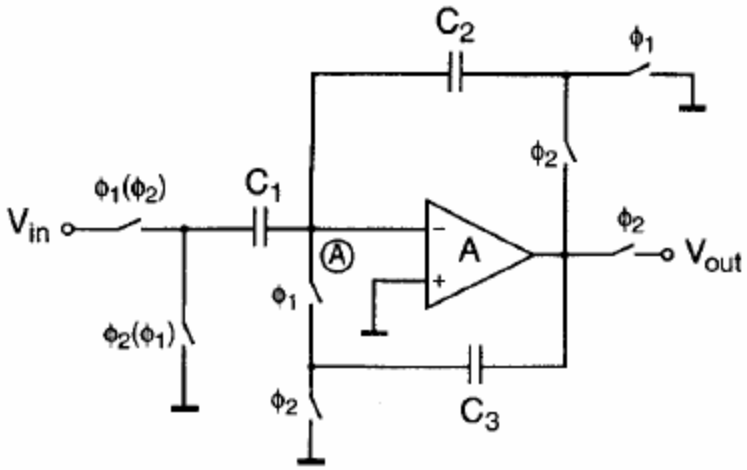
$$v_{n,in}(n) = v_n(n) - v_n(n-1/2);$$

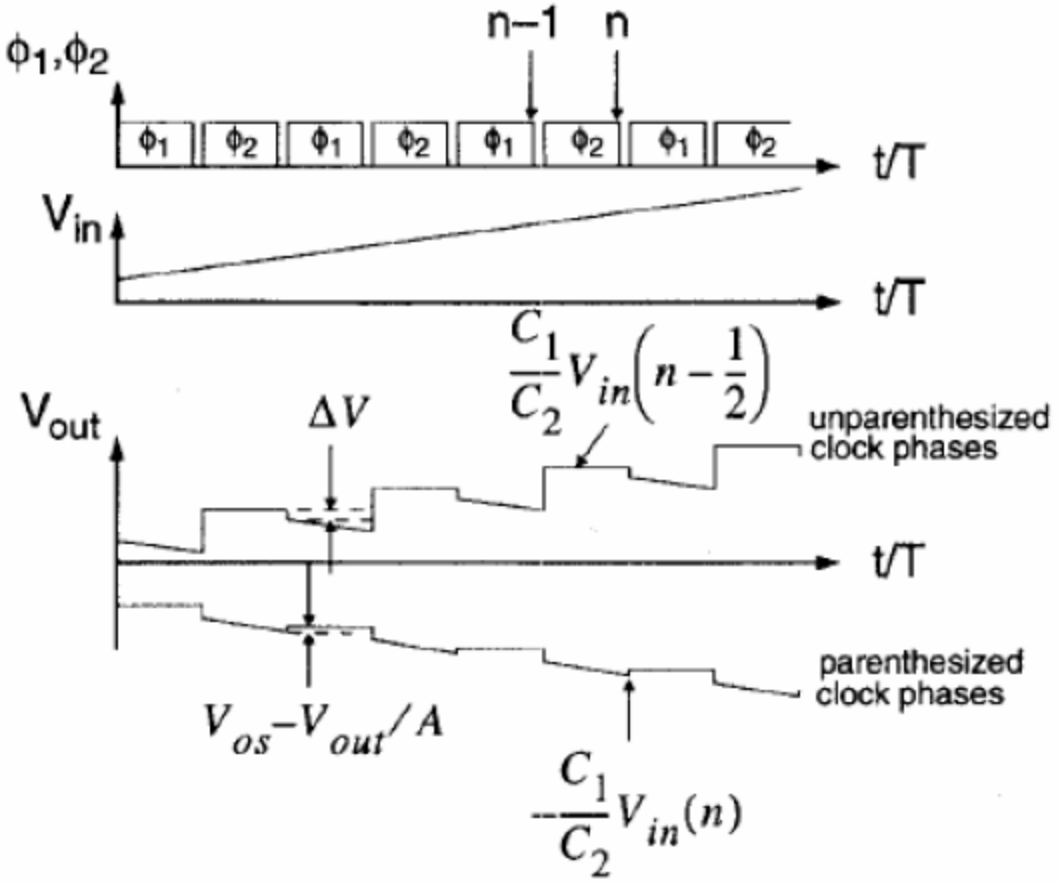
Transfer function without folding: $|H_N|^2 = 4\sin^2(\omega T/4)$

Vos, V1/f and (for oversampled signals) $\mu Vout$ may be reduced by H_N. Here, $\mu Vout$ is not considered, since it is not important for a comparator.

An Offset- and Finite-Gain-Compensated SC Amplifier

Haug et al., 1984 ISCAS





Analysis of Compensated Gain Amplifier

Input-output relation for inverting operation:

$$v_{out}(n) = -C_1/C_2 v_{in}(n) + (1 + C_1/C_2)[v^-(n) - v^-(n-1/2)]$$

The S/H capacitor switches from 0 to

$v^-(n) = V_{os} - \mu v_{out}(n-1/2)$ **as** $\phi_1 \to 1$. **Hence,**

$v_{out}(n-1/2) - v_{out}(n-1) = V_{os} - \mu v_{out}(n-1/2)$ **, where** $\mu = 1/A$ **.**

At low signal frequencies where $v_{out}(n) \cong v_{out}(n-1)$ **,**

the error term is only $(1 + C_1/C_2)\mu^2 v_{out}$ **. The dc gain is**

$$H(1) = \frac{-C_1/C_2}{(1 + C_1/C_2)\mu^2} \bullet +1$$

The output step at reset is only $A_v \cong V_{os} - \mu v_{out} - (C_1/C_3)\Delta v_{in}$ **,**
where the last term enters for noniverting operation only. Av is usually 1~10 mV. The slewing required is minimal. The output offset is $\mu(1 + C_1/C_2)V_{os}$ **.**

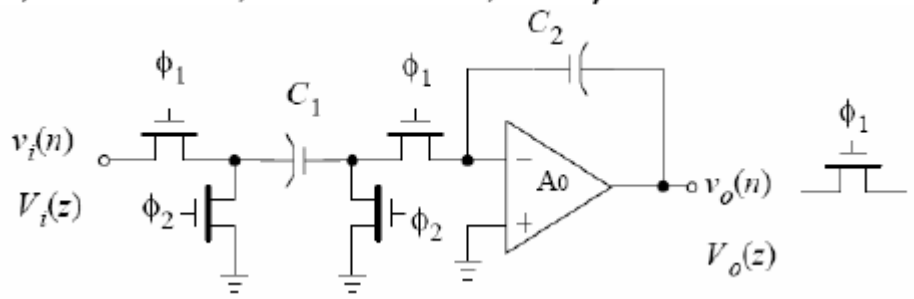
Error in H(1): denom. should have + 1. Clock feedthrough generates some residual offset. Can be used as a compensated delay stage.

Finite Opamp DC Gain Effect

For $A_0 \to \infty$, $H_i(e^{j\omega t}) = \dfrac{-(C_1/C_2)e^{(j\omega T)/2}}{2\sin((\omega T)/2)}$

For $A_0 < \infty$, $H(e^{j\omega t}) = (1+m(\omega))e^{j\theta(\omega)}H_i(e^{j\omega T})$.

Here, the relative gain error $m \cong -(1/A_0)(1+C_1/(2C_2))$
the relative phase error $\theta \cong (C_1/C_2)/(A_0\omega T)$.
(Martin, PhD thesis, U of Toronto, 1980)

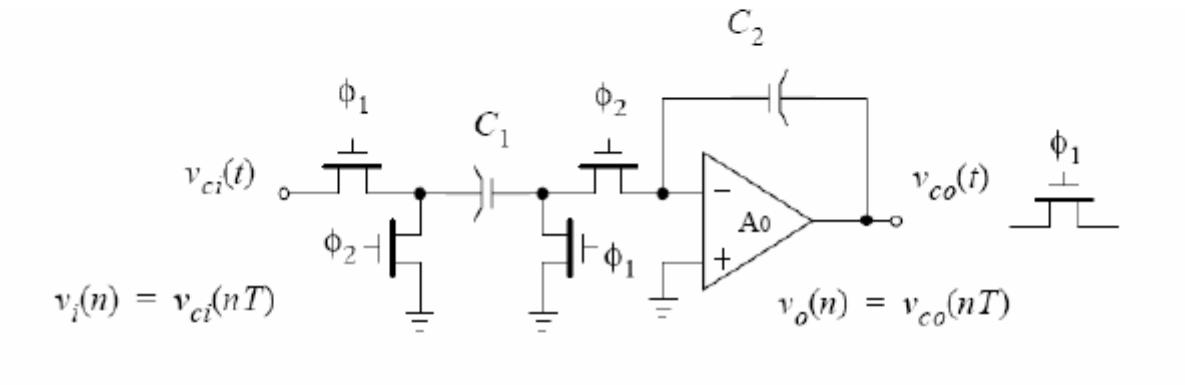


Equations valid only for high frequencies.
At unity-gain freq. ω_i : $2\sin(\omega_i T/2) = C_1/C_2$, $m(\omega_i) \sim \theta(\omega_i) \sim -1/A_0$
Usually, the magnitude error is smaller the (C1/C2) error and is negligible. The phase error shifts poles/zeros horizontally, like dissipation: important!

Finite Opamp DC Gain Effect (Cont'd)

Non-inverting integrator: similar derivation, same $m(\omega), \theta(\omega)$. In a biquad, $s_p \to s_p(1-1/A_0)$ due to $m(\omega)$. The phase errors result in

$$\frac{1}{Q_p} \to \frac{1}{Q_p} + \theta_1(\omega_0) + \theta_2(\omega_0) \sim \frac{1}{Q_p} + \frac{2}{A_0}$$



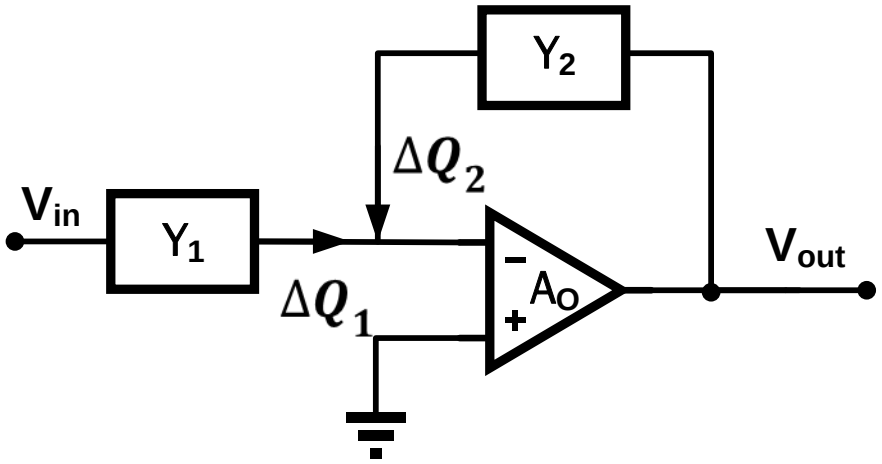
Change in peak gain: $-20\lg(1+2Q_p/A_0)$ (in dB)

can be large for $Q_p >> 1$!

For $Q_p = 15, A_0 = 1000, \Delta G \sim -0.26dB$

High Q_p → use high A_0 opamp! Gain-squaring integrators!

Model for Finite - Gain Effect



$$\Delta Q_i = Y_i(V_i^+ - V_i^-)$$

is the charge flow in one clock period

For $A_O \to \infty, \Delta Q_1 = Y_1 V_{in} = -\Delta Q_2 = -Y_2 V_O$

so H(z) = $V_O / V_{in} = -Y_1 / Y_2$

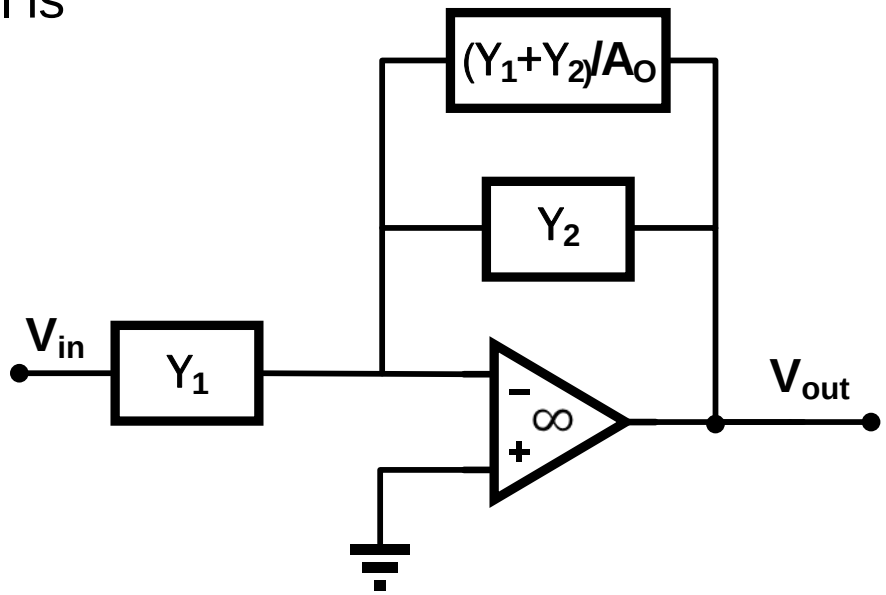
Model for Finite - Gain Effect (Cont'd)

For finite A_O,

$$\Delta Q_1 = Y_1(V_{in} + V_O/A_O) = -Q_2 = -Y_2(V_O + V_O/A_O)$$

$$H(z) = -Y_1/(Y_2 + Y_1/A_O + Y_2/A_O)$$

so the model is



Correlated Level Shifting

R. Gregoire,JSSC, 2008

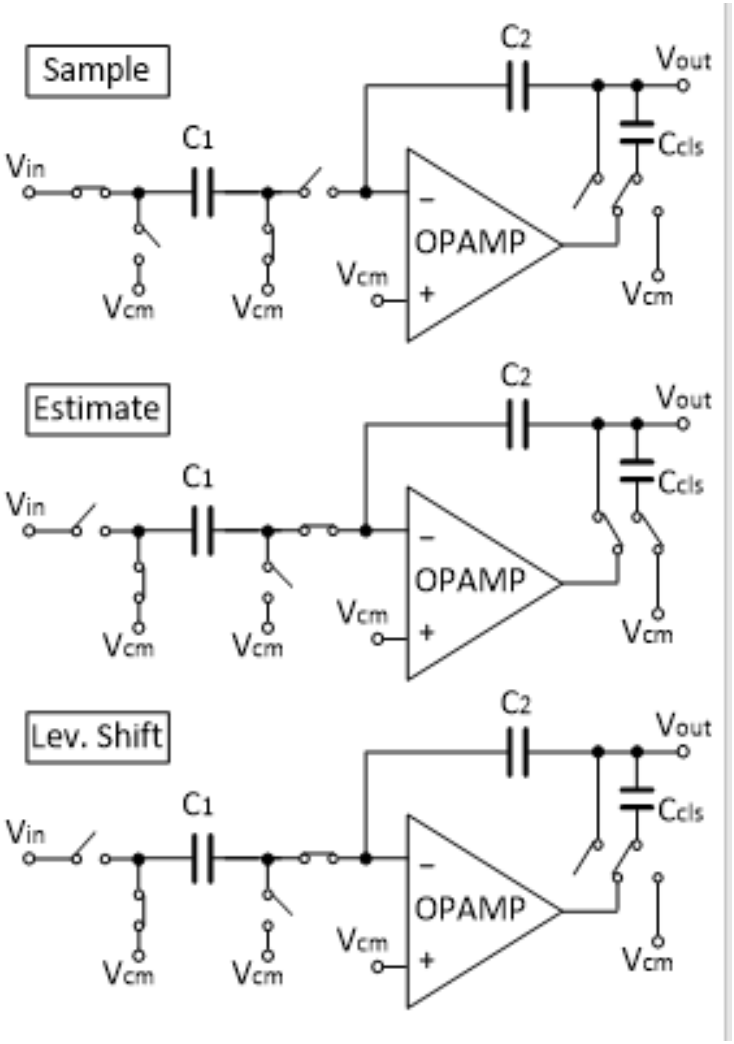
- Additional capacitor (Ccls) at the output of the amplifier
- Working principle (integrator):
  - a) **Sampling phase;**
  - b) **Estimating phase**: coarse integration and charging of Ccls
    - Voltage left in C1:

$$V_{c1(est)} = -\frac{V_{out(est)}}{A}$$

  - c) **Level shifting phase:** connecting Ccls inside the loop, and performing fine integration
    - Voltage left in C1:

$$V_{c1(ls)} = -\frac{V_{out(ls)} - V_{out(est)}}{A}$$

- For two-stage compensated opamp, the compensate cap should be included in the CLS loop.
- Ideally, CLS can boost the DC gain from A to A^2.



Finite Opamp Bandwidth Effect

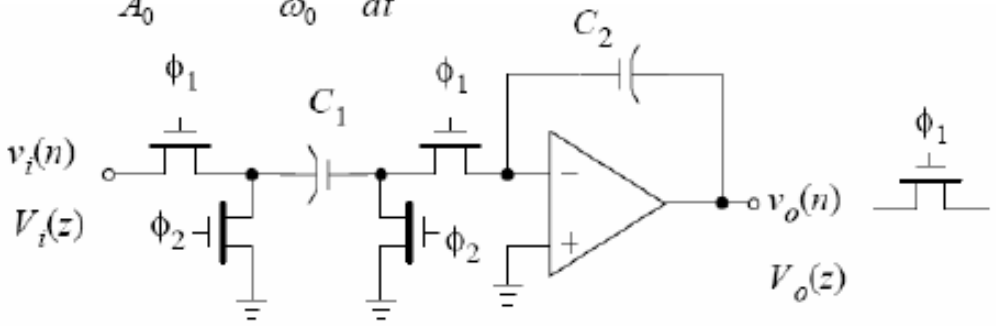
One-pole opamp model:

$$A_v(s) = \frac{-\omega_0}{s - s_1} \approx \frac{-1}{s/\omega_0 + 1/A_0} = \frac{V_o(s)}{V(s)}$$

- ω_o *UNITY GAIN FREQUENCY*

Or, in time domain,

$$\frac{1}{A_0} v_o(t) + \frac{1}{\omega_0}\frac{dv_o(t)}{dt} = -v(t)$$



Combine with KVL, charge conservation. Finding and sampling $v_o(t)$, calculating $V_o(z)/V_i(z)$, and setting $z = e^{j\omega T}$, for an inverting integrator results in

$$m(\omega) = -e^{-k_1}(1 - k\cos\omega T)$$

$$\theta(\omega) = -e^{-k_1} k \sin\omega T$$

Where $k = C_2/(C_1 + C_2)$ is the feedback factor. $k_1 = k\omega_0 T/2 = k\pi f_0/f_c$ should be >>1.

Time constant: $\tau = 1/(k\omega_0)$ should be << T/2.

Finite Opamp Bandwidth Effect (Cont'd)

Since $k_1 = k\pi\omega_0 / \omega_c$, for k~1, if $\omega_0 \geq 5\omega_c$ then $k_1 \geq 15$ and

$e^{-k_1} < 3 \cdot 10^{-7}$, so both m and θ are negligible. Hence, for $C_1 << C_2$, use

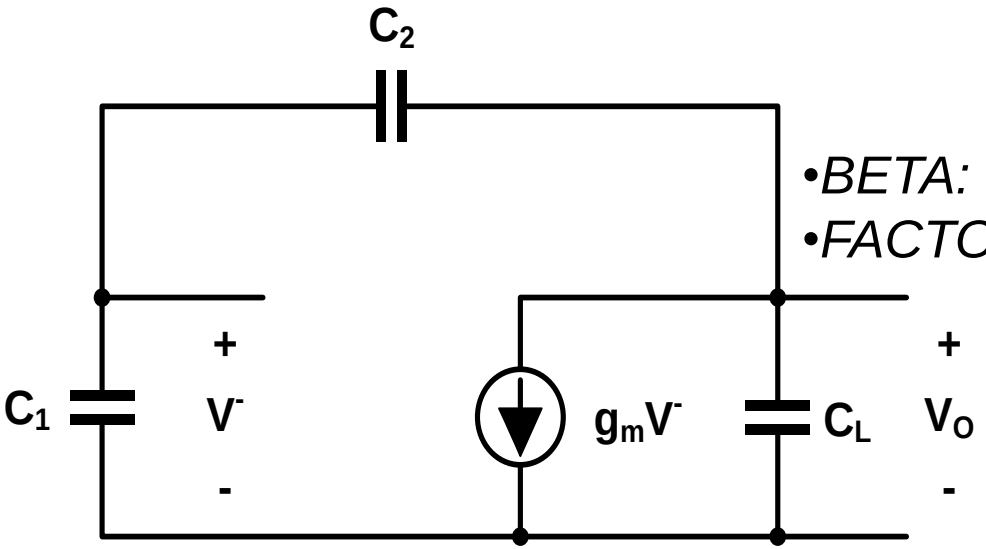
$\omega_0 \geq 5\omega_c$.

•*CLOCK FR. > 20.NYQUIST FREQU. FOR AAF.*

For k < 1, even higher ω_o may be needed. Due to the exponential behavior, the error increases rapidly if ωo is too small!

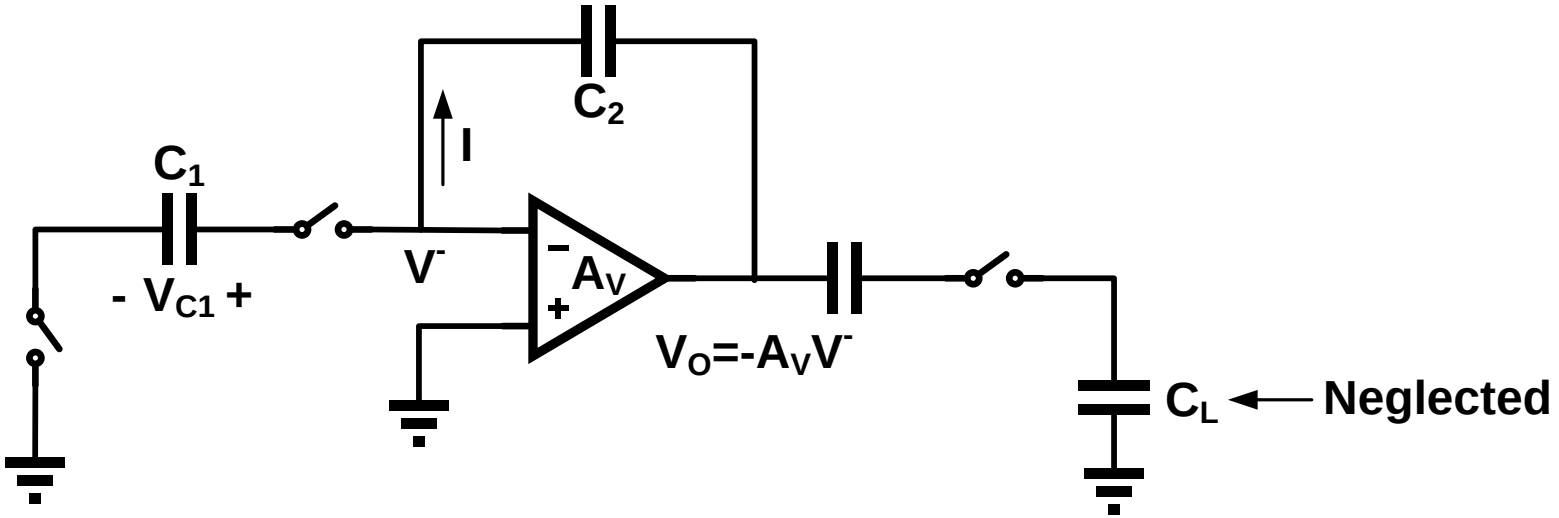
The derivation assumes vin(t) is constant. If several stages settle simultaneously, or if there is a continuous-time loop of opamp and coupling C's, then computer analysis (SWITCAP, Fang/Tsividis) is needed.

Time Constant of OTA-SC Integrator



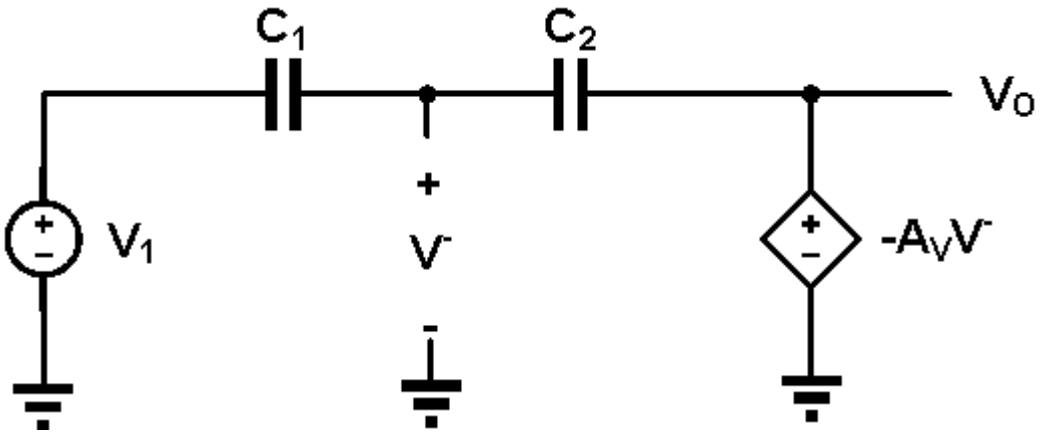
- $V_1 = \beta V_O$ $\quad \beta \triangleq \frac{C_2}{C_1+C_2}$
- *BETA: FEEDBACK FACTOR*
- $V_1 = \frac{-\beta g_m V^-}{s(C_L+C_S)}$
- ***At pole S_P, V_1=V^-***
- $S_p = \frac{-\beta g_m}{C_L+C_S} = \frac{-C_2 g_m}{C_L(C_1+C_2)+C_1C_2}$
- ***Open-loop Gain***
- ***Transient term:***
- $g_m V^- + sC_L V_O + sC_S V_o = 0$
- $e^{s_p t} = e^{-t/\tau}$ $\quad \tau = \frac{1}{|s_p|} = \frac{C_L+C_S}{\beta g_m}$
- $C_S \triangleq \frac{C_1 C_2}{C_1+C_2}$
- ***Unity-gain conventional integrator, assuming all C is equal:***
- $V_o = \frac{-g_m V^-}{s(C_L+C_S)}$
- $\tau = \frac{3C}{g_m}$

Integrator Using a Two-Stage (Buffered) Opamp (VCVS)



- $A_V = \frac{A_0}{s/\omega_p + 1}$
- *Let Initial Values be $V_{C1}=V_1$, $V_{C2}=0$*
- $I = (V_1 - V_O)\frac{sC_1C_2}{C_1+C_2} = sC_2(V^- - V_O)$

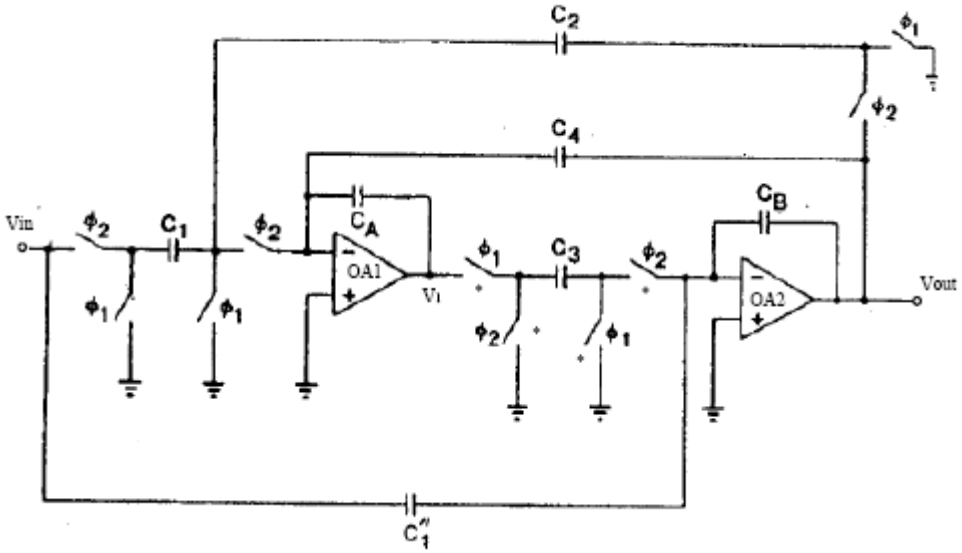
Integrator Using a Two-Stage (Buffer) Opamp



- $V_O = -A_V V^- \cong V_1 \frac{1-\beta}{S/(A_0\omega_p)+\beta+1/A_0}$
- $\beta \triangleq \frac{C_2}{C_1+C_2}$

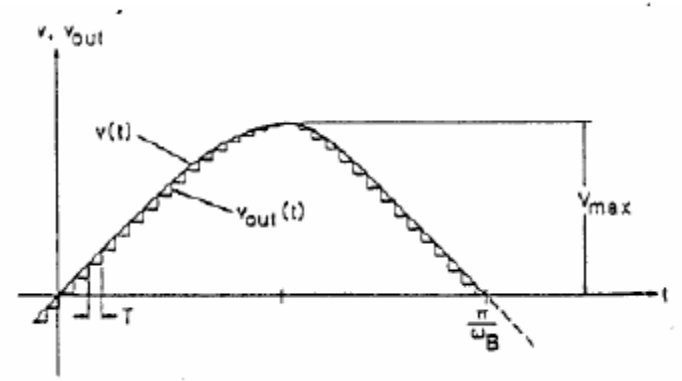
- ***Pole at:*** $-\left(\beta + 1/A_0\right)A_0\omega_p \cong -\beta\omega_u$
- ***Time Constant:*** $\tau \cong 1/\beta\omega_u$
- ***Settling level:*** $V_O(S)|_{s=0} = \frac{1-\beta}{\beta+1/A_0} \cong -\frac{C_1}{C_2}$

High-Q Biquad

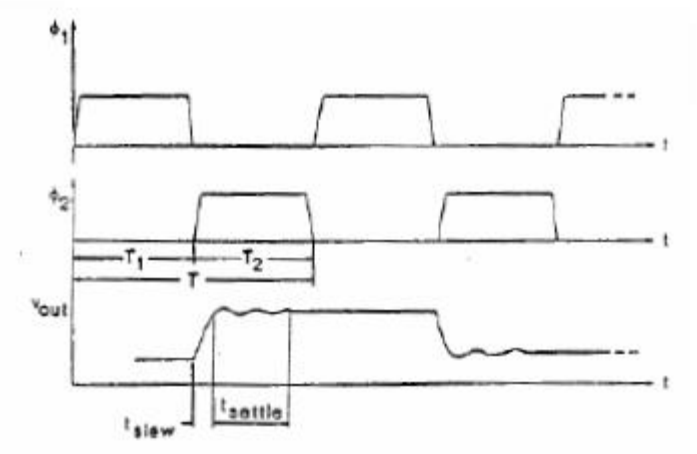


- For original phases, both opamps settle when $\Phi 2 \rightarrow 1$. Changing the $*\Phi 1$, they settle separately. V1 changes twice in one cycles, but OA1 still has the same T/2 time (T for the change at $\Phi 1 \rightarrow 1$.) to settle and to charge C3. The transient when $\Phi 2 \rightarrow 1$ has a full period to settle in OA1 and OA2 .

Slew Rate Estimation (1)



Nonlinear slewing followed by linear settling:



$t_{slew} = xT_2 \sim xT/2$

$S_r = \left|(dv_{out})/(dt)\right|_{\max}$. **For** $v(t) = V_{\max} \sin \omega_B t$ **where** ω_B **is the maximum sine wave freq. at input, the slope** $|dv/dt|$ **of the envelope v(t) is** $\leq \omega_B V_{\max}$. **Then** $S_r \sim 2\omega_B V_{\max}/x$, **very pessimistic estimate!**

Slew Rate Estimation (2)

- Much simpler estimate can be based on assuming that *Cin* is fully discharged in the slewing phase. Then the slew current can be found from

- $I_S \sim C_{in}.V_{in,max}/[x.T/2]$

- Less pessimistic than the previous estimate.

Noise Considerations

- Clock feedthrough from switches
- External noise coupled in from substrate, power lines, etc
- Thermal and 1/f noise generated in switches and opamps

(1) Has components at f=0, fc, can be reduced by dummy switches, differential circuit, etc. May be signal dependent!

(2) Discussed elsewhere.

(3) Thermal noise in MOSFETs: PSD is

$$S_T = \frac{\overline{v_{nT}^2}}{\Delta f} = 4\theta R \quad , \qquad \theta = kT$$

For $f \geq 0$, only (one-sided distribution).

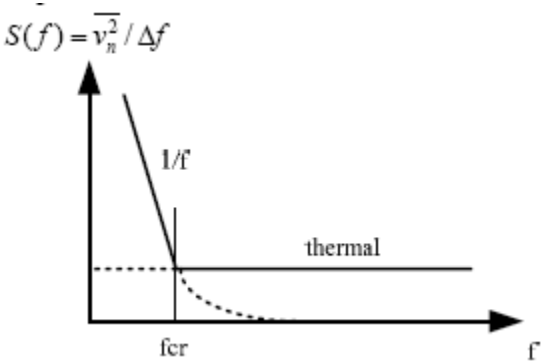
Flicker noise:

$$S_f = \frac{\overline{v_{nT}^2}}{\Delta f} = \frac{k}{C_{ox} W L f}$$

Total noise PSD: $S = S_T + S_f$.

Noise Considerations (Cont'd)

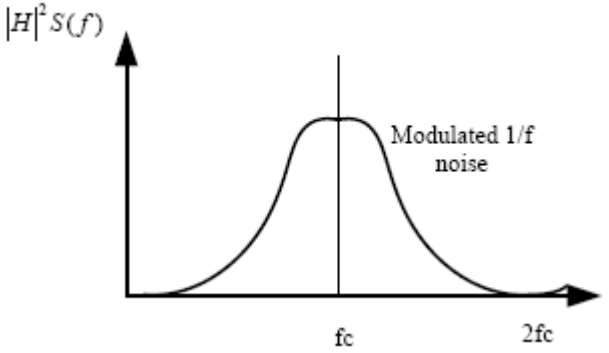
- Noise spectra



- Offset compensation (CDS—correlated double sampling); subtracts noise, T/2 second delayed.

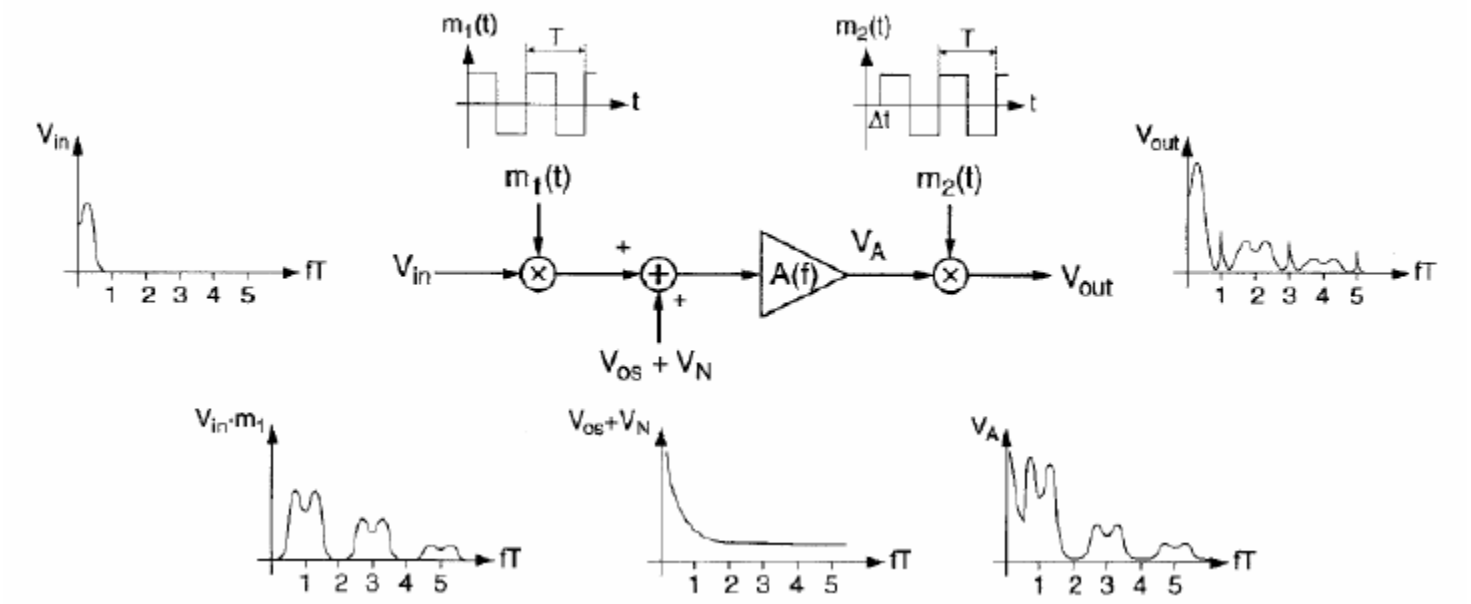
$$H_{CDS} = 1 - e^{-j\omega T/2}$$

$$|H|^2 = 4\sin^2(\omega T/4)$$



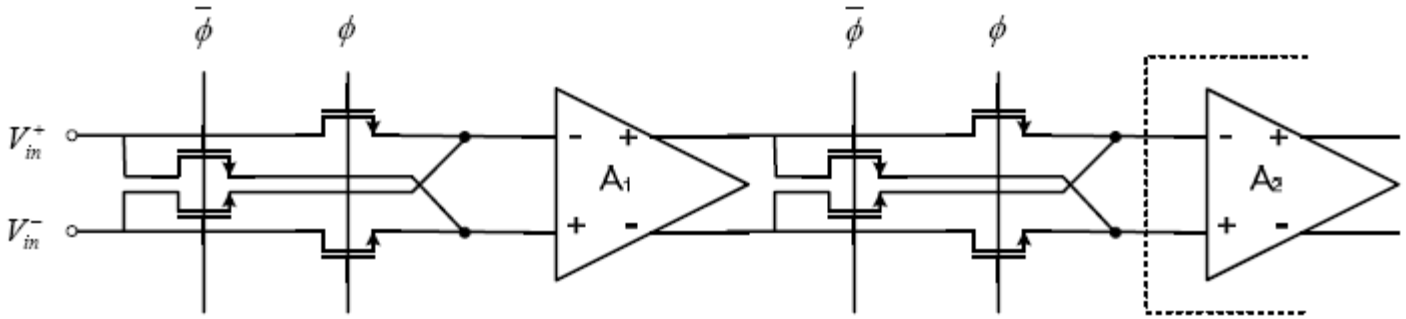
CDS:
1. Pick up noise, no signal;
2. Pick up noise, plus signal;
3. Substract the two.

Chopper Stabilization



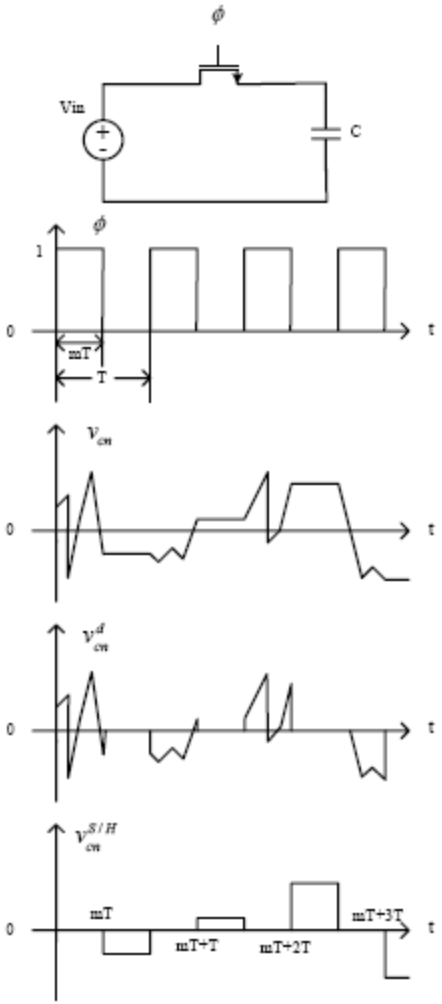
Fully differential circuits needed.

Chopper Stabilization (Cont'd)



Differential SC amplifier using chopping.

Noise Aliasing



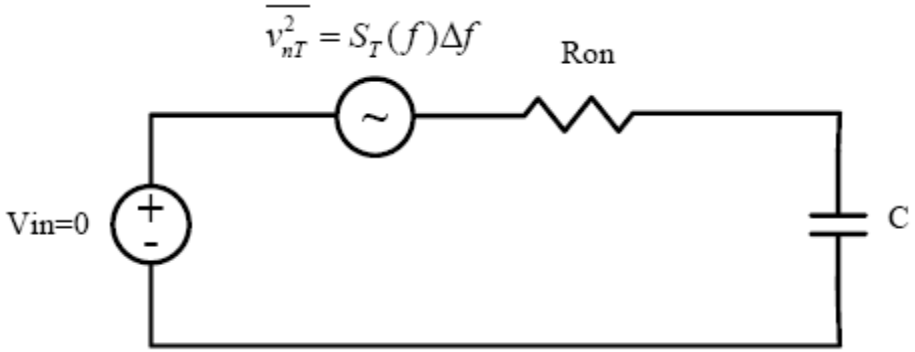
Mean-square values are the same (θ / C) within all windows.

Direct noise power: $\overline{(v_{cn}^{d})^2} = \frac{m\theta}{C}$

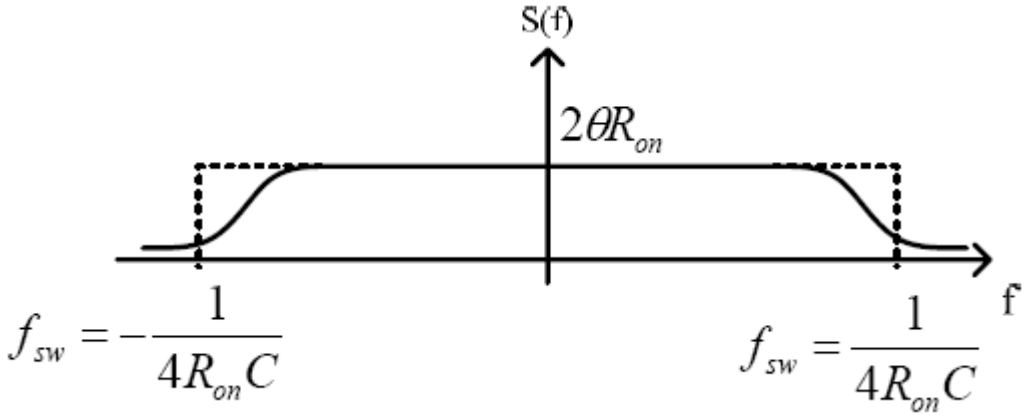
S/H PSD: $\frac{\overline{(v_{cn}^{s/H})^2}}{\Delta f} = \left(\frac{\tau \sin f\tau\pi}{Tf\tau\pi}\right)^2 \cdot \sum_{k=-\infty}^{k=\infty} S(f - kf_c)$

S(f): RC filtered direct noise
Most noise at dc!

Equivalent Circuit for Direct Noise



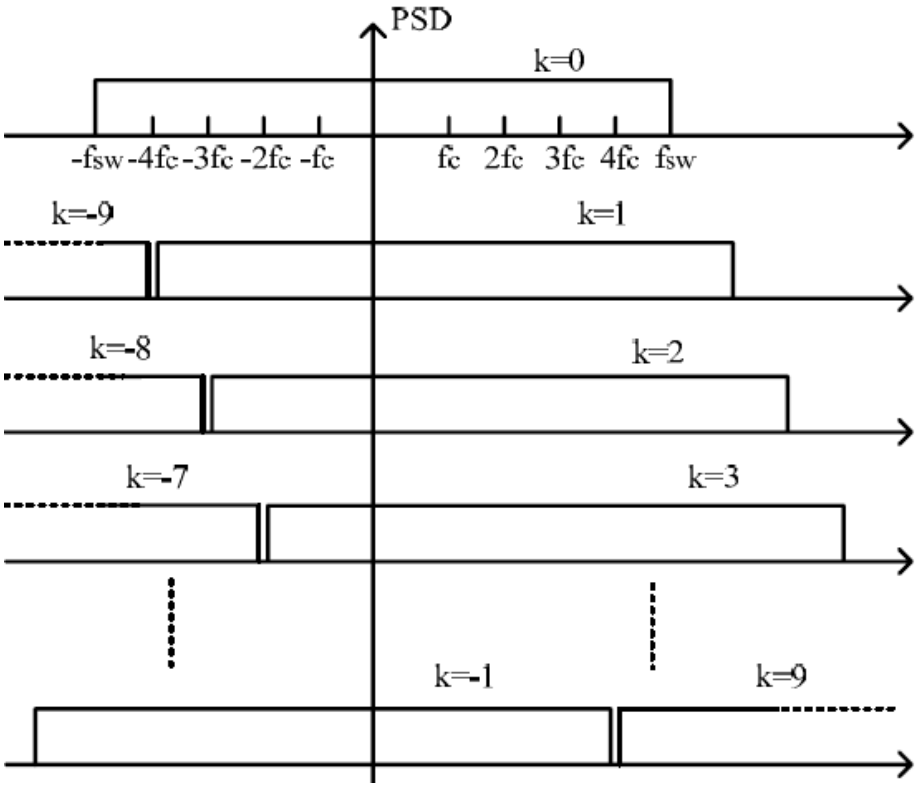
S(f) for direct noise: low-pass filtered and windowed white noise.



For satisfactory settling (0.1%), $R_{on}C \le mT/7 = m/(7f_c)$, $f_{sw} \ge 3.5 f_c$.

Noise Aliasing

Aliasing for $f_{sw} = 5 f_c$



S(f) is magnified by $2f_{sw}/f_c = 10$! The PSD is $\theta/(Cf_c)$ after aliasing (i.e. sampling but not holding).

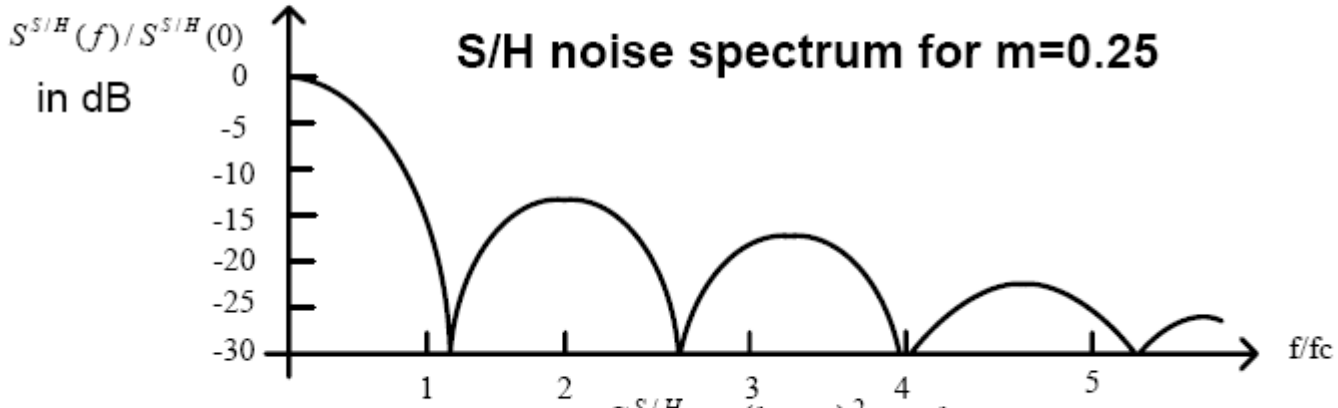
Noise power = kT/C.

Noise Spectra

For low frequencies (f<<fc)

$$S^{S/H}(f) \approx \frac{(1-m)^2\theta}{f_c C}$$ **decreases with m↑**

$$S^{d}(f) \approx 2m\theta R_{on}$$ **increases with m↑**



S/H noise spectrum for m=0.25

Low frequency noise ratio $r = \frac{S^{S/H}}{S^{d}} \approx \frac{(1-m)^2}{2m}\frac{1}{f_c R_{on} C}$

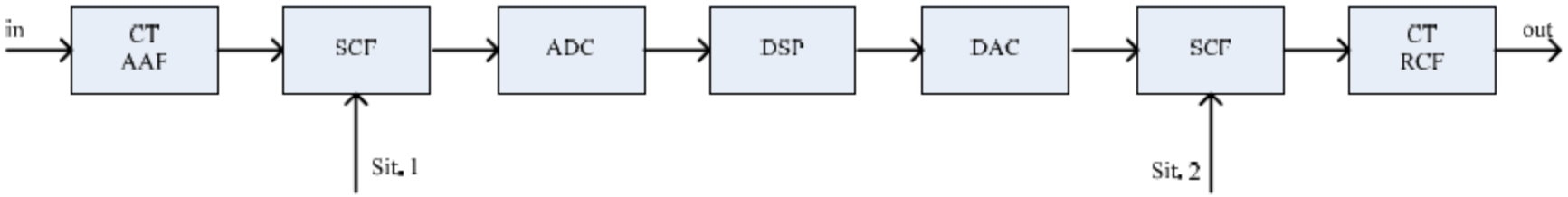
$r \geq 3.5(1/m-1)^2 > 3.5$

For m=0.25, r=31.5!

Noise generated in stage independent of Ron, but the noise generated in preceding stages (direct noise) gets filtered, so the Ron should be as large as possible!

Switched-Capacitor Noise

Two situations; example:



Situation 1: only the sampled values of the output waveform matter; the output spectrum may be limited by the DSP, and hence $V_{RMS,n}$ reduced. Find V_{RMS} from $\sqrt{KTC}$ charges; adjust for DSP effects.

Situation 2: the complete output waveform affects the SNR, including the S/H and direct noise components. Usually the S/H dominates. Reduced by the reconstruction filter.

Calculation of SC Noise (Summary)

- In the switch-capacitor branch, when the switch is on, the capacitor charge noise is lowpass-filtered by Ron and C. The resulting charge noise power in C is kTC. It is a colored noise, with a noisebandwidth fn=1/(4R_{on}C). The low-frequency PSD is 4kTR_{on}.
- When the switch operates at a rate fc<<fn, the samples of the charge noise still have the same power kTC, but spectrum is now white, with a PSD=2kTC/fc. For the situation when only discrete samples of the signal and noise are used, this is all that we need to know.
- For continuous-time analysis, we need to find the powers and spectra of the direct and S/H components when the switch is active. The direct noise is obtained by windowing the filtered charge noise stored in C with a periodic window containing unit pulses of length m/fc. This operation (to a good approximation)
- simply scales the PSD, and hence the noise power, by m. The low-frequncy PSD is thus 4mkTR_{on}.

Calculation of SC Noise (Summary) (Cont'd)

To find the PSD of the S/H noise, let the noise charge in C be sampled and- held at fc, and then windowed by a rectangular periodic window

w(t)=0 for n/fc<t<n/fc+m/fc

w(t)=1 for n/fc+m/fc<t<(n+1)/fc

n=0,1,2,…

Note that is windowing reduces the noise power by (1-m) squared(!), since the S/H noise is not random within each period.

Usually, at low frequencies the S/H noise dominates, since it has approximately the same average power as the direct noise, but its PSD spectrum is concentrated at low frequencies. As a first estimate, its PSD can be estimated at $2(1-m)^2 kT/(f_c C)$ *for frequencies up to fc/2.*